88F6180

Integrated Controller

Hardware Specifications

Doc. No. MV-S104988-U0, Rev. E
December 2, 2008, Preliminary

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.xx

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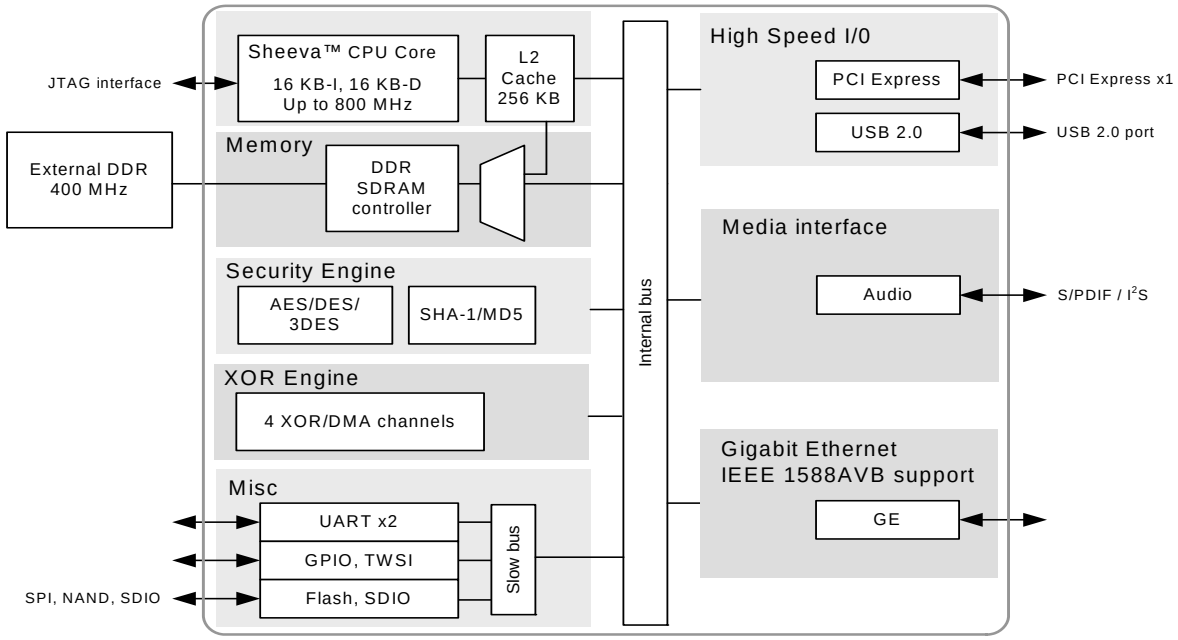
PRODUCT OVERVIEW

The Marvell® 88F6180 is a high-performance, highly integrated controllers. The 88F6180 is based on the Marvell proprietary, ARMv5TE-compliant, high-speed Sheeva™ CPU core The CPU core integrates a 256 KB L2 cache.



88F6180 Functional Block Diagram

FEATURES

- **The 88F6180 includes:**
  - High-performance CPU core, running at up to 800 MHz, with integrated, four-way, set-associative L1 16-KB I-cache/16-KB D-cache and unified, 256-KB, four-way, set-associative L2 cache
  - High-bandwidth dual-port DDR2 memory interface (16-bit DDR2 SDRAM @ up to400 MHz data rate)
  - PCI Express (x1) port with integrated PHY
  - Gigabit Ethernet (10/100/1000 Mbps) MAC
  - USB 2.0 port with integrated PHY
  - Security Cryptographic engine
  - S/PDIF (Sony/Philips Digital Interconnect Format) / I^2S (Integrated Interchip Sound) Audio in/out interface
  - SD/SDIO/MMC interface
  - Two XOR engines, each containing two XOR/DMA channels (a total of four XOR/DMA channels)
  - SPI port with SPI flash boot support
  - 8-bit NAND flash interface with boot support
  - Two 16550 compatible UART interfaces
  - TWSI port
  - 30 multi-purpose pins
  - Internal Real Time Clock (RTC)
  - Interrupt controller
  - Timers
  - 128-bit eFuse (one-time programmable memory)
- **Sheeva™ CPU core**
  - Up to 800 MHz
  - 32-bit and 16-bit RISC architecture
  - Compliant with v5TE architecture, as published in the *ARM Architect Reference Manual*, Second Edition
  - Includes MMU to support virtual memory features
  - 256-KB, four-way, set-associative L2 unified cache
  - 16-KB, four-way, set-associative I-cache
  - 16-KB, four-way, set-associative D-cache
  - 64-bit internal data bus
  - Branch Prediction Unit
  - Supports JTAG/ARM ICE
  - Supports both Big and Little Endian modes
- **DDR2 SDRAM controller**
  - 16-bit interface
  - Up to 200 MHz clock frequency (400 MHz data rate)
  - DDR SDRAM with a clock ratio of 1:N and 2:N between the DDR SDRAM and the CPU core, respectively
  - SSTL 1.8V I/Os
  - Auto calibration of I/Os output impedance
  - Supports two DRAM chip selects
  - Supports all DDR devices densities up to 1 Gb
  - Supports up to 16 open pages (page per bank)
  - Up to 512 MB total address space
  - Supports on-board DDR designs (no DIMM support)
  - Supports 2T mode, to enable high-frequency operation under heavy load configuration
  - Supports DRAM bank interleaving
  - Supports up to a 128-byte burst per single memory access
- **PCI Express interface (x1)**
  - PCI Express Base 1.1 compatible
  - Integrated low-power SERDES PHY, based on proven Marvell® SERDES technology
  - Serves as a Root Complex or an Endpoint port
  - x1 link width
  - 2.5 Gbps data rate
  - Lane polarity reversal support
  - Maximum payload size of 128 bytes
  - Single Virtual Channel (VC-0)
  - Replay buffer support
  - Extended PCI Express configuration space
  - Advanced Error Reporting (AER) support
  - Power management: L0s and software L1 support
  - Interrupt emulation message support
  - Error message support
- **PCI Express master specific features**
  - Single outstanding read transaction
  - Maximum read request of up to 128 bytes
  - Maximum write request of up to 128 bytes
  - Up to four outstanding read transactions in Endpoint mode
- **PCI Express target specific features**
  - Supports up to eight read request transactions
  - Maximum read request size of 4 KB
  - Maximum write request of 128 bytes
  - Supports PCI Express access to all of the controller's internal registers
- **Integrated GbE (10/100/1000) MAC port**
  - Supports 10/100/1000 Mbps
  - Dedicated DMA for data movement between memory and port
  - Priority queuing on receive based on Destination Address (DA), VLAN Tag, and IP TOS
  - Layer 2/3/4 frame encapsulation detection
  - TCP/IP checksum on receive and transmit

- Supports proprietary 200 Mbps Marvell MII (MMII) interface
- Supports RGMII, MII/MMII interface
- DA filtering

■ **Precise Timing Protocol (PTP)**
- Supports precise time stamping for packets, as defined in IEEE 1588 PTP v1 and v2 and IEEE 802.1AS draft standards
- Supports Flexible Time Application interface to distribute PTP clock and time to other devices in the system
- Optionally accepts an external clock input for time stamping

■ **Audio Video Bridging networks**
- Supports IEEE 802.1Qav draft Audio Video Bridging networks
- Supports time- and priority-aware egress pacing algorithm to prevent bunching and bursting effects—suitable for audio/video applications
- Supports Egress Jitter Pacer for AVB-Class A and AVB-Class B traffic and strict priority for legacy traffic queues

■ **USB 2.0 port**
- Serves as a peripheral or host
- USB 2.0 compliant
- Integrated USB 2.0 PHY
- Enhanced Host Controller Interface (EHCI) compatible as a host
- As a host, supports direct connection to all peripheral types (LS, FS, HS)
- As a peripheral, connects to all host types (HS, FS) and hubs
- Up to four independent endpoints, supporting control, interrupt, bulk, and isochronous data transfers
- Dedicated DMA for data movement between memory and port

■ **Cryptographic engine**
- Hardware implementation on encryption and authentication engines, to boost packet processing speed
- Dedicated DMA to feed the hardware engines with data from the internal SRAM memory or from the DDR memory
- Implements AES, DES, and 3DES encryption algorithms
- Implements SHA1 and MD5 authentication algorithms

■ **S/PDIF / I^2S Audio In/Out interface**
- Either S/PDIF or I^2S inputs can be active at one time
- Both S/PDIF and I^2S outputs can be simultaneously active, transferring the same PCM data

■ **S/PDIF-specific features**
- Compliant with 60958-1, 60958-3, and IEC61937 specifications
- Sample rates of 44.1/48/96 kHz
- 16/20/24-bit depths

■ **I^2S-specific features**
- Sample rates of 44.1/48/96 kHz
- I^2S input and I^2S output operate at the same sample rate
- 16/24-bit depths
- I^2S in and I^2S out support independent bit depths (16 bit/24 bit)
- Supports plain I^2S, right-justified and left-justified formats

■ **SD/SDIO/MMC host interface**
- 1-bit/4-bit SDmem, SDIO, and MMC cards
- Up to 50 MHz
- Hardware generate/check CRC, on all command and data transactions on the card bus

■ **Two XOR engines and DMA**
- Two XOR/DMA channels per XOR engine (for a total of four XOR/DMA channels)
- Chaining via linked-lists of descriptors
- Moves data from source interface to destination interface
- Supports increment or hold on both Source and Destination Addresses
- Supports XOR operation, on up to eight source blocks—useful for RAID applications
- Supports iSCSI CRC-32 calculation

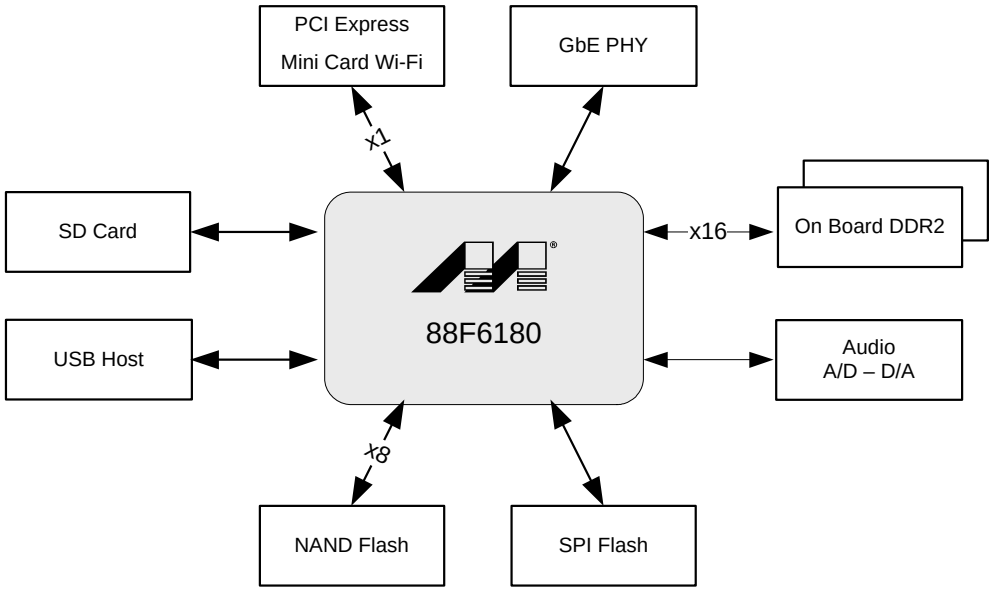
■ **NAND flash controller**
- 8-bit NAND flash interface
- Glueless interface to CE Care and CE Don't Care NAND flash devices
- Boot support

■ **Serial Peripheral Interface (SPI) controller**
- Up to 41.6 MHz clock
- Supports direct boot from external SPI serial flash memory

■ **Two UART Interfaces**
- 16550 UART compatible
- Two pins for transmit and receive operations
- Two pins for modem control functions

■ **Two-Wire Serial Interface (TWSI)**
- General purpose TWSI master/slave port
- Can also be used for serial ROM initialization

- **30 Multi-Purpose Pins dedicated for peripheral functions and general purpose I/O**
  - Each pin can be configured independently.
  - GPIO inputs can be used to register interrupts from external devices, and to generate maskable interrupts.
- **Interrupt Controller**
  Maskable interrupts to CPU core
  (and PCI Express for a PCI Express endpoint)
- **Two general purpose 32-bit timers/counters**
- **Internal architecture**
  - Mbus-L bus for high-performance, low-latency CPU core to DDR SDRAM connectivity
  - Advanced Mbus architecture
  - Dual port DDR SDRAM controller connectivity to both CPU and Mbus
- **Bootable from**
  - SPI flash
  - NAND flash
  - PCI Express
  - UART (for debug purpose)
- **225-pin LFBGA package, 13 ×13 mm, 0.8 mm pitch**



Usage Model Example: Access Point

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Preface

About this Document

This datasheet provides the hardware specifications for the 88F6180 integrated controller. The hardware specifications include detailed pin information, configuration settings, electrical characteristics and physical specifications.

This datasheet is intended to be the basic source of information for designers of new systems.

In this document, the “88F6180” is often referred to as the “device”.

Related Documentation

The following documents contain additional information related to the 88F6180:

- *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*, Doc No. MV-S104860-U0
- *Sheeva™ 88SV131 ARM v5TE Processor Core with MMU and L1/L2 Cache Datasheet*, Doc No. MV-S104950-U0
- *Unified Layer 2 (L2) Cache for Sheeva™ CPU Cores Addendum*, Doc No. MV-S104858-U0
- *88F6180, 88F6190, 88F6192, and 88F6281 Functional Errata, Interface Guidelines, and Restrictions*, Doc No. MV-S501157-U0
- *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*, Doc No. MV-S301398-00[1]
- *AN-63: Thermal Management for Marvell Technology Products* Doc No. MV-S300281-00[1]
- *AN-179: TWSI Software Guidelines for Discovery™, Horizon™, and Feroceon® Devices*, Doc No. MV-S300754-00[1]
- *AN-183: 88F5181 and 88F5281 Big Endian and Little Endian Support*, Doc No. MV-S300767-00[1]
- *AN-260 System Power-Saving Methods for 88F6180, 88F6190, 88F6192, and 88F6281*, Doc No. MV-S301454-00[1]
- *TB-227: Differences Between the 88F6190, 88F6192, and 88F6281 Stepping Z0 and A0*, Doc No. MV-S105223-00[1]
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Doc No. MV-S700019-00
- *ARM Architecture Reference Manual*, Second Edition
- *PCI Express Base Specification*, Revision 1.1
- *Universal Serial Bus Specification*, Revision 2.0, April 2000, Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips
- *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 0.95, November 2000, Intel Corporation
- *ARC USB-HS OTG High-Speed Controller Core reference V 4.0.1*
- Federal Information Processing Standards (FIPS) 46-2 (Data Encryption Standard)
- FIPS 81 (DES Modes of Operation)
- FIPS 180-1 (Secure Hash Standard)
- FIPS draft - Advanced Encryption Standard (Rijndeal)
- RFC 1321 (The MD5 Message-Digest Algorithm)

1. This document is a Marvell proprietary, confidential document, requiring an NDA and can be downloaded from the Marvell Extranet.

- RFC 1851 – The ESP Triple DES Transform
- RFC 2104 (HMAC: Keyed-Hashing for Message Authentication).
- RFC 2405 – The ESP DES-CBC Cipher Algorithm With Explicit IV
- IEEE standard, 802.3-2000 Clause 14
- ANSI standard X3.263-1995

See the Marvell Extranet website for the latest product documentation.

Document Conventions

The following conventions are used in this document:

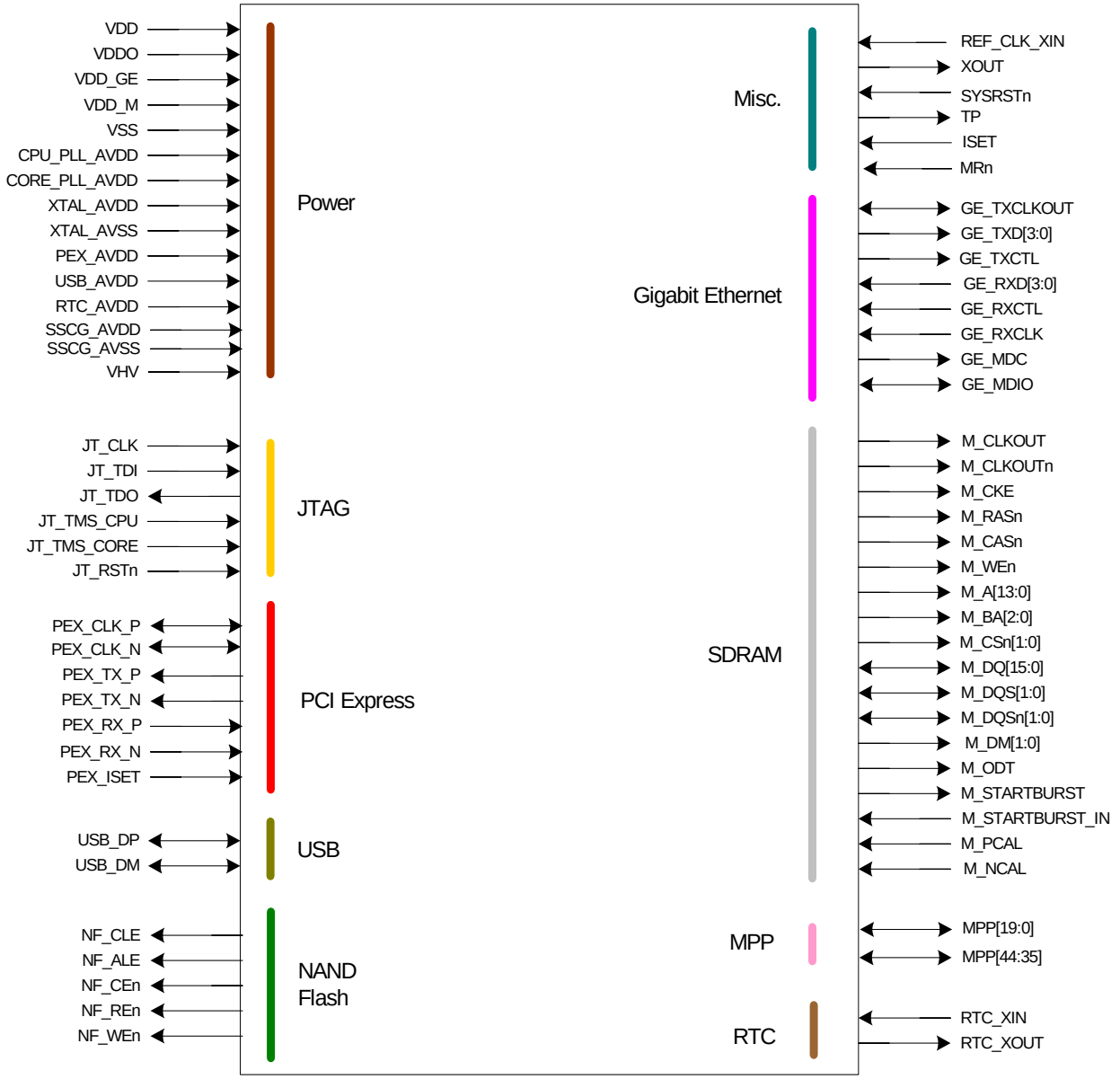
Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte Gb: gigabit GB: gigabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Pin and Signal Descriptions

This section provides the pin logic diagram for the 88F6180 device and a detailed description of the pin assignments and their functionality.

1.1 Pin Logic

Figure 1: 88F6180 Pin Logic Diagram



NOTE: The GE_TXCLKOUT pin is an input only when used as the MII/MMII Transmit Clock.
The MPP interface consists of pin MPP[19:0] and MPP[44:35].
The pins MPP[34:20] do not exist.

For details about MPP configuration options see Section 4.1, Multi-Purpose Pins Functional Summary, on page 41.

1.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Table 1<Default ¬¹ Font> defines the abbreviations and acronyms used in the pin description tables.

Table 1: Pin Functions and Assignments Table Key

Term	Definition
[n]	n - Represents the SERDES pair number
<n>	Represents port number when there are more than one ports
Analog	Analog Driver/Receiver or Power Supply
Calib	Calibration pad type
CML	Common Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
DDR	Double Data Rate
GND	Ground Supply
HCSL	High-speed Current Steering Logic
I	Input
I/O	Input/Output
O	Output
o/d	Open Drain pin The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
Power	VDD Power Supply
SSTL	Stub Series Terminated Logic for 1.8V
t/s	Tri-State pin
XXXn	n - Suffix represents an Active Low Signal

Table 2: Interface Pin Prefix Codes

Interface	Prefix
Misc	N/A
DDR SDRAM	M_
PCI Express	PEX_
Gigabit Ethernet	GE_
USB 2.0	USB_
JTAG	JT_
RTC	RTC_

Table 2: Interface Pin Prefix Codes (Continued)

Interface	Prefix
NAND Flash	NF_
MPP	N/A
TWSI	TW_
UART	UA_
Audio	AU_
SPI	SPI_
SDIO	SD_
PTP	PTP_

1.2.1 Power Supply Pins

Table 3 provides the voltage levels for the various interface pins. These do not include the analog power supplies for the PLLs or PHYs which are explicitly mentioned in the other pin description tables.

Table 3: Power Pin Assignments

Pin Name	I/O	Pin Type	Description
VDD	I	Power	1.0V Digital core and CPU voltage
VDDO	I	Power	3.3V I/O power for MPP[44:36], MPP[19:0] and JTAG pins
VDD_GE	I	Power	1.8V or 3.3V I/O supply voltage for RGMII and SMI interfaces 3.3V I/O supply voltage for MII/MMII and SMI interfaces **NOTE:** When configure to RGMII mode at 3.3V, only 10/100 Mbps operation is supported.
VDD_M	I	Power	1.8V I/O supply voltage for the DDR2 SDRAM interface
VSS	I	GND	VSS
CPU_PLL_AVDD	I	Power	1.8V analog quiet power to CPU PLL **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
CPU_PLL_AVSS	I	GND	CPU PLL ground
CORE_PLL_AVDD	I	Power	1.8V analog quiet power to Core PLL **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
SSCG_AVDD	I	Power	1.8V quiet power supply to the internal Spread Spectrum Clock Generator
SSCG_AVSS	I	GND	Ground for the internal Spread Spectrum Clock Generator
XTAL_AVDD	I	Power	1.8V analog quiet power to on-chip clock inverter for supporting external crystal, and on-chip current reference for USB PHYs **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
VHV	I	Power	I/O supply voltage for eFuse: • 2.5V for eFuse burning only • 1.0V for eFuse reading only
PEX_AVDD	I	Power	PCI Express PHY quiet power supply 1.8V **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendations.
USB_AVDD	I	Power	USB 2.0 PHY quiet 3.3V power supply **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for power supply filtering recommendation.
RTC_AVDD	I	Power	1.5V (via battery) or 1.8V (via the board) RTC interface voltage

1.2.2 Miscellaneous Pin Assignment

The Miscellaneous signal list contains clock and reset, test, and related signals.

Table 4: Miscellaneous Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
REF_CLK_XIN	I	Analog	XTAL_AVDD	Reference clock input from external oscillator or input from external crystal. Used as input to core, CPU, and USB PLLs.
XOUT	O	Analog	XTAL_AVDD	XTAL_OUT Feedback signal to external crystal. When not used, leave this pin floating.
SYSRSTn	I	CMOS	VDDO	System reset Main reset signal of the device clock. Used to reset all units to their initial state. When in the reset state, most output pins are in Tri-State.
SYSRST_OUTn	O	CMOS	VDDO	Reset request from the device to the board reset logic. This pin is multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).
PEX_RST_OUTn	O	CMOS	VDDO	Optional PCI Express Endpoint card reset output This pin is multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).
TP	O	Analog		Analog Test Point for USB, and PCI Express interfaces For internal use. Leave this pin unconnected.
ISET	I	Analog		USB_ISET (output): Current Reference Pull down to VSS through a 6.04 kΩ pull-down resistor. See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended resistor value.
MRn	I	CMOS	VDD_GE	Active-Low, Manual Reset Input SYSRST_OUTn is asserted low as long as the MRn input signal is asserted low, and for additional 20 ms after MRn (manual reset) de-assertion This pin is internally pulled up.
NC				Reserved for Marvell¬Æ future usage. Leave unconnected externally.

1.2.3 DDR SDRAM Interface Pin Assignments

Table 5: DDR SDRAM Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
M_CLKOUT M_CLKOUTn	O	SSTL	VDD_M	SDRAM Differential Clock Pair
M_CKE	O	SSTL	VDD_M	Driven high to enable SDRAM clock. Driven low when setting the SDRAM to Self-refresh mode.
M_RASn	O	SSTL	VDD_M	SDRAM Row Address Select Asserted to indicate an active ROW address driven on the SDRAM address lines.
M_CASn	O	SSTL	VDD_M	SDRAM Column Address Select Asserted to indicate an active column address driven on the SDRAM address lines.
M_WEn	O	SSTL	VDD_M	SDRAM Write Enable Asserted to indicate a write command to the SDRAM.
M_A[13:0]	O	SSTL	VDD_M	SDRAM Address Driven during RASn and CASn cycles to generate—together with M_BA[2:0]—the SDRAM address.
M_BA[2:0]	O	SSTL	VDD_M	Driven during M_RASn and M_CASn cycles to select one of the eight SDRAM virtual banks. **NOTE:** If an SDRAM device does not support the BA[2] pin, leave the M_BA[2] unconnected.
M_CSn[1:0]	O	SSTL	VDD_M	SDRAM Chip Selects Asserted to select a specific SDRAM Physical bank.
M_DQ[15:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Bus Driven during write. Driven by SDRAM during reads.
M_DQS[1:0], M_DQSn[1:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Strobe Driven by the 88F6180 during write. Driven by SDRAM during reads.
M_DM[1:0]	O	SSTL	VDD_M	SDRAM Data Mask Asserted by the 88F6180 to select the specific byte out of the 16-bit data to be written to the SDRAM.
M_ODT	O	SSTL	VDD_M	SDRAM On Die Termination control. Driven high to connect the SDRAM on die termination. Driven low to disconnect the SDRAM's termination. **NOTE:** For the recommended setting, refer to the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*.

Table 5: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
M_STARTBURST	O	SSTL	VDD_M	Start Burst 88F6180 indication of starting a burst read transaction. Asserted with the first M_CASn cycle of SDRAM access. **NOTE:** Must be routed on board to the SDRAM, and back to the 88F6180 as M_STARTBURST_IN. For the recommended length calculation for this routing and termination requirements, see the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*.
M_START BURST_IN	I	SSTL	VDD_M	Start Burst Input
M_PCAL	I	Calib		SDRAM interface P channel output driver calibration. Connect to VSS through a resistor. The resistor value can vary between 30–70 ohm. **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended values of the calibration resistors.
M_NCAL	I	Calib		SDRAM interface N channel output driver calibration. Connect to M_VDD through a resistor. The resistor value can vary between 30–70 ohm. **NOTE:** See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended values of the calibration resistors.

1.2.4 PCI Express Interface Pin Assignments

Table 6: PCI Express Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
PEX_CLK_P/N	I/O	HCSL	PEX_AVDD	PCI Express Reference Clock 100 MHz, differential This clock can be configured as input or output according to the reset strap (see Table 28, Reset Configuration, on page 52). **NOTE:** For Output mode, 50-ohm, pull-down resistors are required.
PEX_TX_P/N	O	CML	PEX_AVDD	Transmit Lane Differential pair of PCI Express transmit data
PEX_RX_P/N	I	CML	PEX_AVDD	Receive Lane Differential pair of PCI Express receive data
PEX_ISET	I	Analog		Current reference. Pull down to VSS through a 5 kΩ resistor. See the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide* for the recommended resistor value.

1.2.5 Gigabit Ethernet Port Interface Pin Assignments

Table 7: Gigabit Ethernet Port Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GE_TXCLKOUT	t/s O	CMOS	VDD_GE	RGMII Transmit Clock RGMII transmit reference output clock for GE_TXD[3:0] and GE_TXCTL Provides 125 MHz, 25 MHz or 2.5 MHz clock.
	I			MII/MMII Transmit Clock MII/MMII transmit reference clock from PHY. Provides the timing reference for the transmission of the MII transmit clock, transmit enable, and GE_TXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
GE_TXD[3:0]	t/s O	CMOS	VDD_GE	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate with bits [3:0] driven on the rising edge of GE_TXCLKOUT and bits [7:4] driven on the falling edge.
				MII/MMII Transmit Data Contains the transmit data nibble outputs that are synchronous to the transmit clock input.
GE_TXCTL	t/s O	CMOS	VDD_GE	RGMII Transmit Control Transmit control synchronous to the GE_TXCLKOUT output rising/falling edge. GE_TXEN is driven on the rising edge of GE_TXCLKOUT. A logical derivative of transmit enable and transmit error is driven on the falling edge of GE_TXCLKOUT.
				MII/MMII Transmit Error It is synchronous to transmit clock. Multiplexed on MPP
GE_RXD[3:0]	I	CMOS	VDD_GE	RGMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input rising/falling edge.
				MII/MMII Receive Data Contains the receive data nibble inputs that are synchronous to GE_RXCLK input.
GE_RXCTL	I	CMOS	VDD_GE	RGMII Receive Control GE_RXCTL is presented on the rising edge of GE_RXCLK. A logical derivative of receive data valid and receive data error is presented on the falling edge of RXCLK.
				MII/MMII Receive Data Valid

Table 7: Gigabit Ethernet Port Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GE_RXCLK	I	CMOS	VDD_GE	RGMII Receive Clock The receive clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock derived from the received data stream.
				MII/MMII Receive Clock Provides the timing reference for the reception of the receive data valid, receive error, and GE_RXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.

1.2.6 Serial Management Interface (SMI) Interface Pin Assignments

Table 8: Serial Management Interface (SMI) Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GE_MDC	t/s O	CMOS/	VDD_GE	Management Data Clock MDC is derived from TCLK divided by 128. Provides the timing reference for the transfer of the MDIO signal.
GE_MDIO	t/s I/O	CMOS	VDD_GE	Management Data In/Out Used to transfer control and status information between PHY devices and the GbE controller. **NOTE:** A pull-up is required.

1.2.7 USB 2.0 Interface Pin Assignments

Table 9: USB 2.0 Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
USB_DP USB_DM	I/O	CML	USB_AVDD	USB 2.0 Data Differential Pair

1.2.8 JTAG Interface Pin Assignment

Table 10: JTAG Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
JT_CLK	I	CMOS	VDDO	JTAG Clock Clock input for the JTAG controller. **NOTE:** This pin is internally pulled down to 0.
JT_RSTn	I	CMOS	VDDO	JTAG Reset When asserted, resets the JTAG controller. **NOTE:** This pin is internally pulled down to 0.[1]
JT_TMS_CPU	I	CMOS	VDDO	CPU JTAG Mode Select Controls CPU JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TMS_CORE	I	CMOS	VDDO	Core JTAG Mode Select Controls the Core JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TDO	O	CMOS	VDDO	JTAG Data Out Driven on the falling edge of JT_CLK.
JT_TDI	I	CMOS	VDDO	JTAG Data In JTAG serial data input. Sampled with the JT_CLK rising edge. **NOTE:** This pin is internally pulled up to 1.

1. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP (Test Access Port) can be reset by driving the JT_TMS signal HIGH for 5 JT_CLK cycles.

1.2.9 Real Time Clock (RTC) Interface Pin Assignments

Table 11: RTC Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
RTC_XIN	I	Analog	RTC_AVDD	RTC Crystal Clock Input
RTC_XOUT	O	Analog	RTC_AVDD	RTC Crystal Clock Feedback

1.2.10 NAND Flash Interface Pin Assignment

Table 12: NAND Flash Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
NF_IO[7:0]	I/O	CMOS	VDDO	Data Input/Output Used to output command, address and data, and to input data during read operations. **NOTE:** All of the NF_IO pins are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41)
NF_CLE	O	CMOS	VDDO	Command Latch Enable Controls the activating path for commands sent to the command register.
NF_ALE	O	CMOS	VDDO	Address Latch Enable Controls the activating path for the address to the internal address registers.
NF_CEn	O	CMOS	VDDO	Chip Enable Controls the device selection.
NF_REn	O	CMOS	VDDO	Read Enable Controls the serial data-in.
NF_WEn	O	CMOS	VDDO	Write Enable Controls writes to the NF_IO[7:0] ports.

1.2.11 MPP Interface Pin Assignment

Table 13: MPP Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
MPP[19:0]	t/s I/O	CMOS	VDDO	Multi Purpose Pin Various functionalities
MPP[35]	t/s I/O	CMOS	VDD_GE	Multi Purpose Pin Various functionalities **NOTE:** When VDD_GE receives 1.8V power (for RGMII), this pin can be used as a GPIO signal of 1.8V (unlike the other GPIO pins, which are 3.3V).
MPP[44:36]	t/s I/O	CMOS	VDDO	Multi Purpose Pin Various functionalities

Note

The various functionalities of the MPP pins are detailed in Section 4, Pin Multiplexing, on page 41.

1.2.12 Two-Wire Serial Interface (TWSI) Interface

Note All of the TWSI signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).

Table 14: Two-Wire Serial Interface (TWSI) Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
TW_SDA	o/d I/O	CMOS	VDDO	TWSI Port Serial Data Address or write data driven by the TWSI master or read response data driven by the TWSI slave. **NOTE:** Requires a pull-up resistor to VDDO.
TW_SCK	o/d I/O	CMOS	VDDO	TWSI Port Serial Clock Serves as output when acting as an TWSI master. Serves as input when acting as an TWSI slave. **NOTE:** Requires a pull-up resistor to VDDO.

1.2.13 UART Interface

Note

All of the UART signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).

Table 15: UART Port 0/1 Interface Pin Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
UA0/1_RXD	I	CMOS	VDDO	UART Port RX Data
UA0/1_TXD	O	CMOS	VDDO	UART Port TX Data
UA0/1_CTS	I	CMOS	VDDO	Clear to Send
UA0/1_RTS	O	CMOS	VDDO	Request to Send

1.2.14 Audio (S/PDIF / I²S) Interface

Note

- All of the Audio signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).
- If the Audio interface is not used, leave all of the signals unconnected.
- The Audio signals are powered on VDDO or on VDD_GE_B, based on the pin multiplexing option.

Table 16: Audio (S/PDIF / I²S) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
AU_SPDIFI	I	CMOS	VDD_GE	S/PDIF In
AU_SPDIFO	O	CMOS	VDD_GE	S/PDIF Out
AU_ SPDFRMCLK	O	CMOS	VDD_GE	S/PDIF Recovered Master Clock (256 x F_S)[1] For the frequency of this clock, see the Audio External Reference Clock section of Table 40, Reference Clock AC Timing Specifications, on page 69.
AU_I2SBCLK	O	CMOS	VDD_GE	I^2S Bit Clock (64 x F_S)
AU_I2SDO	O	CMOS	VDD_GE	Transmitter Data Out
AU_I2SLRCLK	O	CMOS	VDD_GE	I^2S Left/Right Clock (1 x F_S)
AU_I2SMCLK	O	CMOS	VDD_GE	I^2S Master Clock (256 x F_S)
AU_I2SDI	I	CMOS	VDD_GE	I^2S Receiver Data In
AU_EXTCLK	I	CMOS	VDD_GE	External Audio Clock For the frequency of this clock, see the Audio External Reference Clock section of Table 40, Reference Clock AC Timing Specifications, on page 69.

1. F_S is the audio sample rate.

1.2.15 Serial Peripheral Interface (SPI) Interface

Note

All of the SPI signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).

Table 17: Serial Peripheral Interface (SPI) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
SPI_MOSI[1]	O	CMOS	VDDO	SPI Data Output Data is output from the master and input to the slave.
SPI_MISO[2]	I	CMOS	VDDO	SPI Data Input Data is input to the master and output from the slave.
SPI_SCK	O	CMOS	VDDO	SPI Clock
SPI_CSn	O	CMOS	VDDO	SPI Chip Select **NOTE:** This pin requires an external pull up.

1. MOSI = Master Out Slave In.
2. MISO = Master In Slave Out.

1.2.16 Secure Digital Input/Output (SDIO) Interface

Note All of the SDIO signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).

Table 18: Secure Digital Input/Output (SDIO) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
SD_CLK	O	CMOS	VDDO	SDIO Clock
SD_CMD	I/O	CMOS	VDDO	SDIO Command Used to transfer a command serially from the SDIO host to the SDIO device. Used to transfer a command response serially from the SDIO device to the SDIO host. **NOTE:** This pin requires a pull up on board.
SD_D[3:0]	I/O	CMOS	VDDO	SDIO Data Input/Output Used to transfer data from the SDIO host to the SDIO device or vice versa. **NOTE:** These pins require a pull up on board.

1.2.17 Precise Timing Protocol (PTP) Interface

Note

All of the PTP signals are multiplexed on the MPP pins (see Section 4, Pin Multiplexing, on page 41).

Table 19: Precise Timing Protocol (PTP) Interface Signal Assignment

Pin Name	I/O	Pin Type	Power Rail	Description
PTP_CLK	I	CMOS	VDDO	PTP Clock
PTP_EVENT_REQ	I	CMOS	VDDO	Trigger generation to the PTP core.
PTP_TRIG_GEN	O	CMOS	VDDO	Trigger generated by the PTP core.

1.3 Internal Pull-up and Pull-down Pins

Some pins of the device package are connected to internal pull-up and pull-down resistors. When these pins are Not Connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is 50 kΩ. An external resistor with a lower value can override this internal resistor.

Table 20: Internal Pull-up and Pull-down Pins

Pin Name	Pin Number	Pull up/Pull down
GE_TXD[0]	H02	Pull down
GE_TXD[1]	H01	Pull down
GE_TXD[2]	H03	Pull up
GE_TXD[3]	J03	Pull up
GE_TXCTL	J01	Pull down
GE_MDC	L02	Pull up
JT_TMS_CORE	R12	Pull up
JT_RSTn	P10	Pull down
JT_TDI	P11	Pull up
JT_TMS_CPU	N10	Pull up
NF_ALE	P05	Pull up
NF_REn	R06	Pull down
NF_CLE	R05	Pull down
NF_CEn	N07	Pull up
NF_WEn	R07	Pull up
MRn	G03	Pull up
MPP[1]	P03	Pull down
MPP[2]	N02	Pull down
MPP[3]	P02	Pull down
MPP[4]	P01	Pull up
MPP[5]	R03	Pull up
MPP[7]	N05	Pull up
MPP[10]	R04	Pull down

2 Unused Interface Strapping

Table 21 lists the signal strapping to be used for systems in which some of the device interfaces are unused (not connected).

Table 21: Unused Interface Strapping

Unused Interface	Strapping
Ethernet SMI	Pull up GE_MDIO.
MPP	Configure any unused MPP pin to GPIO output. Leave the power supply connected to 3.3V.
USB	Discard the power filter. Leave USB_AVDD connected to 3.3V. All other signals can be left unconnected.
PCI Express	Discard the analog power filters. Leave PEX_AVDD connected to 1.8V. Pull down the PEX_CLK_N signal through a 50 kΩ resistor to GND. Pull up the PEX_CLK_P signal through a 16 kΩ resistor to 1.8V. All other signals can be left unconnected. Configure the PEX_CLK_P and PEX_CLK_N signals as inputs, as indicated in Table 28, Reset Configuration, on page 52.
RTC	Connect RTC_AVDD, RTC_XIN, and RTC_XOUT to GND.
SSCG	Discard the power filter. Leave SSCG_AVDD connected to 1.8V.
eFuse	Connect VHV to VDD

3 88F6180 Pin Map and Pin List

The 88F6180 pin list is provided as an Excel file attachment.

To open the attached Excel pin list file, double-click the pin icons below:

88F6180 BGA Pin Map and Pin List

Note

File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.

4 Pin Multiplexing

4.1 Multi-Purpose Pins Functional Summary

The 88F6180 device contains 30 Multi-Purpose Pins (MPP)—MPP[19:0] and MPP[44:35]. The MPP range is not consecutive. Each one can be assigned to a different functionality through the MPP Control register.

- General Purpose pins: MPP[5:0], MPP[19:7], and MPP[44:35]:
  - GPIO (input/output): MPP[0], MPP[4], MPP[9:8], MPP[9], MPP[11], MPP[17:13], and MPP[44:35]
  - GPO (output): MPP[3:1], MPP[5], MPP[7], MPP[10], MPP[12], and MPP[19:18]
- SYSRST_OUTn: Reset request from the device to the board reset logic. This pin is an output. SYSRST_OUTn is the default setting for MPP[6].
- PEX_RST_OUTn: Optional PCI Express Endpoint card reset output.
- NF_IO[7:0] (NAND Flash data [7:0])
- SPI interface: SPI_MOSI, SPI_MISO, SPI_SCK, SPI_CSn
- UART interface: Transmit and receive functions: UA0/1_TXD, UA0/1_RXD, and Modem control functions: UA0/1_RTSn, UA0/1_CTSn
- SDIO interface: SD_CLK, SD_CMD, SD_D[3:0]
- Audio interface signals: AU_SPDIFI, AU_SPDIFO, AU_SPDIFRMCLK, AU_I2SBCLK, AU_I2SDO, AU_I2SLRCLK, AU_I2SMCLK, AU_I2SDI, AU_EXTCLK
- PTP signals: PTP_EVENT_REQ, PTP_TRIG_GEN, PTP_CLK
- TWSI signals: TW_SDA, TW_SCK

MPP pins can be assigned to different functionalities through the MPP Control register (see Table 22).

Table 22: MPP Functionality

MPP[19:0]	MPP[44:35]
GPIO	GPIO
NAND flash	Audio
TWSI	MII
UART	
SPI	
PTP	
SDIO	

Table 23 lists the functionality of the MPP pins, as determined by the MPP Multiplex register, see the Pins Multiplexing Interface Registers section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

Table 23: MPP Function Summary

Pin name	0x0	0x1	0x2	0x3	0x4	0xC	0xD
MPP[0]	GPIO[0] (in/out)	NF_IO[2] (in/out)	SPI_SCn (out)	-	-	-	-
MPP[1]	GPO[1] (out only)	NF_IO[3] (in/out)	SPI_MOSI (out)	-	-	-	-
MPP[2]	GPO[2] (out only)	NF_IO[4] (in/out)	SPI_SCK (out)	-	-	-	-
MPP[3]	GPO[3] (out only)	NF_IO[5] (in/out)	SPI_MISO (in)	-	-	-	-
MPP[4]	GPIO[4] (in/out)	NF_IO[6] (in/out)	UA0_RXD (in)	-	-	-	PTP_CLK (in)
MPP[5]	GPO[5] (out only)	NF_IO[7] (in/out)	UA0_TXD (out)	-	PTP_TRIG_ GEN (out)	-	-
MPP[6]	-	SYSRST_O UTn (out)	SPI_MOSI (out)	PTP_TRIG_ GEN (out)	-	-	-
MPP[7]	GPO[7] (out only)	PEX_RST_ OUTn (out)	SPI_SCn (out)	PTP_TRIG_ GEN (out)	-	-	-
MPP[8]	GPIO[8] (in/out)	TW_SDA (in/out)	UA0_RTS (out)	UA1_RTS (out)	-	PTP_CLK (in)	MII0_COL (in)
MPP[9]	GPIO[9] (in/out)	TW_SCK (in/out)	UA0_CTS (in)	UA1_CTS (in)	-	PTP_EVEN T_REQ (in)	MII0_CRS (in)
MPP[10]	GPO [10] (out only)	-	SPI_SCK (out)	UA0_TXD (out)	-	PTP_TRIG_ GEN (out)	-
MPP[11]	GPIO[11] (in/out)	-	SPI_MISO (in)	UA0_RXD (in)	PTP_EVEN T_REQ (in)	PTP_TRIG_ GEN (out)	PTP_clk (in)
MPP[12]	GPO[12] (out only)	SD_CLK (out)	-	-	-	-	-
MPP[13]	GPIO[13] (in/out)	SD_CMD (in/out)	-	UA1_TXD (out)	-	-	-
MPP[14]	GPIO[14] (in/out)	SD_D[0] (in/out)	-	UA1_RXD (in)	-	-	MII0_COL (in)
MPP[15]	GPIO[15] (in/out)	SD_D[1] (in/out)	UA0_RTS (out)	UA1_TXD (out)	-	-	-
MPP[16]	GPIO[16] (in/out)	SD_D[2] (in/out)	UA0_CTS (in)	UA1_RXD (in)	-	-	MII0_CRS (in)
MPP[17]	GPIO[17] (in/out)	SD_D[3] (in/out)	-	-	-	-	-

Table 23: MPP Function Summary (Continued)

Pin name	0x0	0x1	0x2	0x3	0x4	0xC	0xD
MPP[18]	GPO[18] (out only)	NF_IO[0] (in/out)	-	-	-	-	-
MPP[19]	GPO[19] (out only)	NF_IO[1] (in/out)	-	-	-	-	-
MPP[35]	GPIO[35] (in/out)	-	-	-	-	MII0_RXERR (in)	-
MPP[36]	GPIO[36] (in/out)	-	-	-	AU_SPDIFI (in)	-	-
MPP[37]	GPIO[37] (in/out)	-	-	-	AU_SPDIFO (out)	-	-
MPP[38]	GPIO[38] (in/out)	-	-	-	AU_SPDIFRMCLK (out)	-	-
MPP[39]	GPIO[39] (in/out)	-	-	-	AU_I2SBCLK (out)	-	-
MPP[40]	GPIO[40] (in/out)	-	-	-	AU_I2SDO (out)	-	-
MPP[41]	GPIO[41] (in/out)	-	-	-	AU_I2SLRCLK (out)	-	-
MPP[42]	GPIO[42] (in/out)	-	-	-	AU_I2SMCLK (out)	-	-
MPP[43]	GPIO[43] (in/out)	-	-	-	AU_I2SDI (in)	-	-
MPP[44]	GPIO[44] (in/out)	-	-	-	AU_EXTCLK (in)	-	-

Note

- For MPPs assigned as NAND flash and SPI flash, wake-up mode after reset depends on Boot mode (see the Boot Device field in Table 28, Reset Configuration, on page 52):
  - When Boot mode is NAND Flash, MPP[5:0] and MPP[19:18] wake up after reset in NAND Flash mode.
  - When Boot mode is SPI Flash, MPP[3:0] wake up after reset in SPI mode.
- Pin MPP[6] wakes up after reset in 0x1 mode (SYSRST_OUTn)
- Pin MPP[7] wakes up after reset:
  - As SPI_CSn, if the boot device—selected according to boot device reset strapping—is 0x2 (boot from SPI flash, SPI_CSn on MPP[7]).
  - As PEX_RST_OUTn, if the boot device—selected according to boot device reset strapping—is any option other than 0x2.
- When TWSI serial ROM initialization is enabled (see TWSI Serial ROM Initialization in Table 28, Reset Configuration, on page 52), MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively.
- All other MPP interface pins wake up after reset in 0x0 mode (GPIO/GPO) and are default set to Data Output disabled (Tri-State). Therefore, those MPPs that are GPIO are in fact inputs, and those that are GPO are Tri-State.
- The SPI interface can be configured using one of the following sets of MPP pins:
  - MPP[3:0]
  - MPP[11], MPP[10], MPP[7], and MPP[6]
  - MPP[3:1] and MPP[7]
- Do not configure *both* MPP[3] and MPP[11] as SPI_MISO. UART0 and UART1 signals are duplicated on a few MPPs. The UART0 or UART1 signals must not be configured to more than one MPP. Some of the MPP pins are sampled during SYSRSTn de-assertion to set the device configuration. These pins must be set to the correct value during reset (see Section 6.5, Pins Sample Configuration, on page 51).
- Pins that are left as GPIO and are not connected should be set to output after SYSRSTn de-assertion.

4.2 Gigabit Ethernet (GbE) Pins Multiplexing on MPP

The 88F6180 has 14 dedicated pins for its GbE port. (12 RGMII pins, an MDC pin, and an MDIO pin).

For the 88F6180, additional GbE interface pins are multiplexed on the MPPs, to serve as the remaining pin interfaces to an external PHY or switch:

- RGMII
- MII/MMII

Table 24 summarizes the GbE port pins multiplexing for the 88F6180.

Table 24: 88F6180 Ethernet Ports Pins Multiplexing

Pin Name	RGMII	MII/MMII
GE_TXCLKOUT	RGMII0_TXCLKOUT (out)	MII0_TXCLK (in)
GE_TXD[3:0]	RGMII0_TXD[3:0] (out)	MII0_TXD[3:0] (out)
GE_TXCTL	RGMII0_TXCTL (out)	MII0_TXEN (out)
GE_RXD[3:0]	RGMII0_RXD[3:0] (in)	MII0_RXD[3:0] (in)
GE_RXCTL	RGMII0_RXCTL (in)	MII0_RXDV (in)
GE_RXCLK	RGMII0_RXCLK (in)	MII0_RXCLK (in)
MPP[35]	NA	MII0_RXERR (in)
MPP[8] or MPP[14]	NA	MII0_COL (in)
MPP[9] or MPP[16]	NA	MII0_CRS (in)

Note When using Gigabit Ethernet signals on MPPs, all relevant Gigabit Ethernet signals (except those marked as NA) must be implemented. For example, if using MII, and the chosen PHY does not have an MII_RXERR out signal, the MII_RX_ERR (in) (MPP[35]) must still be configured accordingly and must have a pull-down resistor.

5 Clocking

Table 25 lists the clocks in the 88F6180.

Table 25: 88F6180 Clocks

Clock Type	Description
CPU PLL	• Reference clock: REF_CLK_XIN (25 MHz) • Derivative clocks: - CPU clock - L2 cache clock - DDR Clock (the Mbus-L uses the DDR clock.) **NOTE:** See Table 28, Reset Configuration, on page 52 for CPU, L2 cache and DDR frequency configuration. L2 cache clock frequency must be equal or higher then DDR clock frequency. If the SSCG enable bit in the Sampled at Reset register is set, then the SSCG circuit is applied for the CPU PLL reference clock (refer to the Sampled at Reset register in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*).
Core PLL	• Reference clock: REF_CLK_XIN (25 MHz) • Derivative clocks: - TCLK (core clock, 166 MHz) - SDIO Clock (100 MHz) - Gigabit Ethernet Clock (125 MHz) - SPI clock (TCLK/30–TCLK/4 MHz) - SMI clock (TCLK/128 MHz) - TWSI clock (up to TCLK/1600) **NOTE:** See Table 28, Reset Configuration, on page 52 for TCLK frequency configuration.
PEX PHY	There are two options for the reference clock configuration, depending on the PCI Express clock 100 MHz differential clock: • The device uses an external source for PCI Express clock. The PEX_CLK_P pin is an input. • The device uses an internal generated clock for PCI Express clock. The PEX_CLK_P pin is an output, driving out the PCI Express differential clock.
USB PHY PLL	• Reference clock: REF_CLK_XIN (25 MHz)

Table 25: 88F6180 Clocks (Continued)

Clock Type	Description
RTC	• Reference clock: RTC_XIN (32.768 kHz) Used for real time clock functionality, see the Real Time Clock section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
PTP	• Reference clock: PTP_CLK (125 MHz) The PTP_CLK can be used for the following functions: • PTP time stamp clock Two options for reference clock: - PTP_CLK - Gigabit Ethernet Clock (125 MHz) • TS unit clock Two options for reference clock: - PTP_CLK/2 - Core PLL • Audio unit clock Two options for reference clock: - PTP_CLK - REF_CLK_XIN (25 MHz) For clocking configuration registers, see the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

The following table lists the supported combinations of the CPU_CLK Frequency select, CPU_CLK to DDR CLK ratio, and to CPU_CLK to CPU L2 clock ratio (see Section 6.5, Pins Sample Configuration, on page 51).

Table 26: Supported Clock Combinations

DDR Clock (MHz)	CPU to DDR Clock Ratio	CPU Clock (MHz)	CPU to L2 Clock Ratio	L2 Clock (MHz)
200	3:1	600	2:1	300
200	4:1	800	2:1	400

5.1 Spread Spectrum Clock Generator (SSCG)

The SSCG (Spread Spectrum Clock Generator) may be used to generate the spread spectrum clock for the PLL input. See SSCG Disable in Table 28, Reset Configuration, on page 52, for SSCG enable/bypass configuration settings.

The SSCG block can be configured to perform up spread, down spread and center spread.

The modulation frequency is configurable. Typical frequency is 30 kHz.

The spread percentage can also be configured up to 1%.

For additional details, see the SSCG Configuration Register description in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

6 System Power Up/Down and Reset Settings

This section provides information about the device power-up/down sequence and configuration at reset.

6.1 Power-Up/Down Sequence Requirements

6.1.1 Power-Up Sequence Requirements

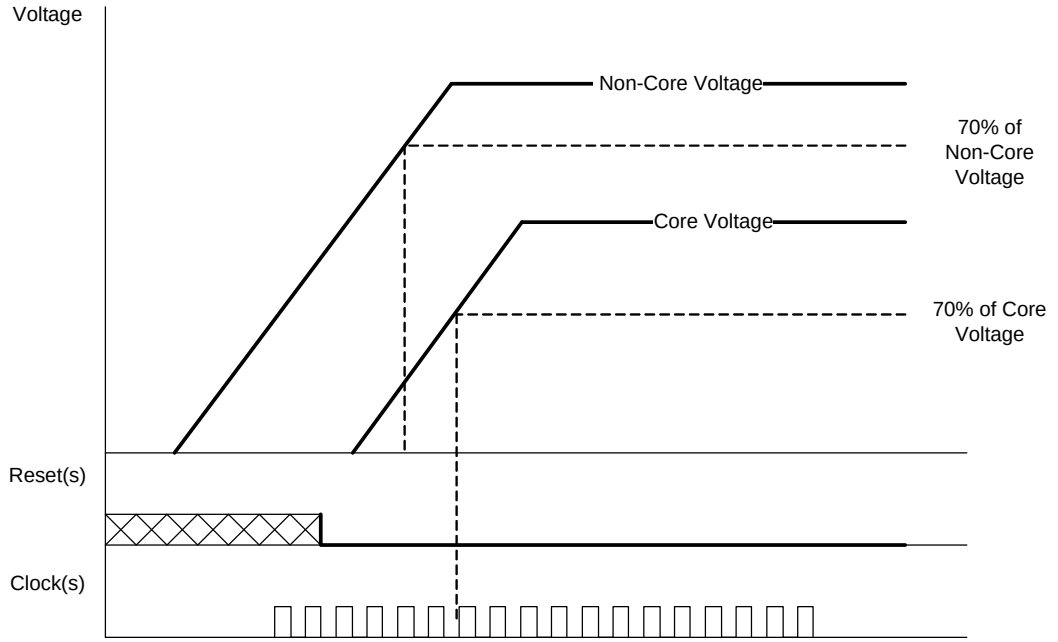
These guidelines must be applied to meet the 88F6180 device power-up requirements:

- The non-core voltages (I/O and Analog) as listed in Table 27 must reach 70% of their voltage level before the core voltages reach 70% of their voltage level.
  The order of the power-up sequence between the non-core voltages is unimportant so long as the non-core voltages power up before the core voltages reach 70% of their voltage level (shown in Figure 2).
- The reset signal(s) must be asserted before the core voltages reach 70% of their voltage level (shown in Figure 2).
- The reference clock(s) inputs must toggle with their respective voltage levels before the core voltages reach 70% of their voltage level (shown in Figure 2).
- If VHV is set to burning mode (2.5V), which is a higher voltage than the VDD voltage, VDD must be powered before VHV, to prevent the fuse from being accidentally burned.

Table 27: I/O and Core Voltages

Non-Core Voltages		Core Voltages
I/O Voltages	**Analog Power Supplies**	
VDD_GE VDD_M VDDO	CPU_PLL_AVDD CORE_PLL_AVDD PEX_AVDD RTC_AVDD SSCG_AVDD XTAL_AVDD USB_AVDD	VDD

Figure 2: Power-Up Sequence Example



Note

- It is the designer's responsibility to verify that the power sequencing requirements of other components are also met.
- Although the non-core voltages can be powered up any time before the core voltages, allow a reasonable time limitation (for example, 100 ms) between the **first** non-core voltage power-up and the **last** core voltage power-up.

6.1.2 Power-Down Sequence Requirements

There are no special requirements for the core supply to go down before non-core power, or for reset assertion when powering down (except for VHV, as described below). However, allow a reasonable time limitation (no more than 100 ms) between the **first** and **last** voltage power-down.

When using the eFuse in Burning mode, VHV must be powered down before VDD.

6.2 Hardware Reset

The device has one reset input pin—SYSRSTn. When asserted, the entire chip is placed in its initial state. Most outputs are placed in high-z, except for the following output pins, that are still active during SYSRSTn assertion:

- M_CLKOUT, M_CLKOUTn
- M_CKE
- M_ODT
- M_STARTBURST
- SYSRST_OUTn

Note Reset (SYSRSTn signal) must be active for a minimum length of 5 ms. core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.

6.2.1 Reset Out Signal

The device has an optional SYSRST_OUTn output signal, multiplexed on an MPP pin, that is used as a reset request from the device to the board reset logic. SYSRST_OUTn is the default option for that MPP pin.

This signal is asserted low for 20 ms, when one of the following **maskable** events occurs:

- Received hot reset indication from the PCI Express link (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Reset register section of the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*).
- PCI Express link failure (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register.
- Watchdog timer expiration and bit <WDRstOutEn> is set to 1 in the RSTOUTn Mask Register.
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register.

This signal is asserted low for 20 ms, when one of the following **non-maskable** events occurs:

- Power on reset (The device includes a power-on-reset (POR) circuit for VDD power.)
- SYSRST_OUTn is asserted low as long as the MRn input signal is asserted low and for an additional 20 ms after MRn de-assertion. (This is useful for implementations that include a manual reset button.)

6.2.2 Power On Reset (POR)

The SYSRST_OUTn output signal is asserted low for 20 ms, when the power-on-reset (POR) circuit is triggered.

POR is triggered when VDD power up (digital core voltage) reaches a VDD threshold (threshold maximum value 0.8V).

Hysteresis: Another trigger will only occur after the power first drops to 50 mV, and then a power up occurs.

6.2.3 SYSRSTn Duration Counter

When SYSRSTn is asserted low, a SYSRSTn duration counter is running.

- The counter clock is the 25 MHz reference clock.
- It is a 29-bit counter, yielding a maximum counting duration of 2^29/25 MHz (21.4 seconds).
- The host software can read the counter value and reset the counter.
- When the counter reach its maximum value, it remains at this value until counter reset is triggered by software.

Note The SYSRSTn duration counter is useful for implementing manufacturer/factory reset. Upon a long reset assertion, greater than a pre-configured threshold, the host software may reset all settings to the factory default values.

6.3 PCI Express Reset

6.3.1 PCI Express Root Complex Reset

As a Root Complex, the device may generate a Hot Reset to the PCI Express port. Upon CPU setting the PCI Express Control register's <conf_mstr_hot_reset> bit, the PCI Express unit sends a Hot Reset indication to the Endpoint, see the PCI Express Interface section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

6.3.2 PCI Express Endpoint Reset

When a Hot Reset packet is received:

- A maskable interrupt is asserted.
- If the <conf_dis_hot_rst_reg_rst> field in the PCI Express Debug Control register is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if not masked by the <conf_msk_hot_reset> field in the PCI Express Debug Control register.

Link failure is detected if the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected:

- A maskable interrupt is asserted.
- If the <conf_dis_link_fail_reg_rst> field in the PCI Express Debug Control register is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if the <conf_msk_link_fail> field is not masked by PCI Express Debug Control register.

Both link fail and hot reset conditions trigger a chip internal reset (if not masked in the PCI Express interface). All the chip logic is reset to the default values, except for sticky registers and the sample on reset logic. In addition, these events can trigger reset to the board, using one of the following:

- PEX_RST_OUTn signal (multiplexed on MPP).
- SYSRST_OUTn output (multiplexed on MPP)—if not masked by the <PexRstOutEn> bit.

The external reset logic (on the board) may assert the SYSRSTn input pin and reset the entire chip.

6.4 Sheeva™ CPU TAP Controller Reset

The Sheeva™ CPU Test Access Port (TAP) controller is reset when JT_RSTn is set and JT_TMS_CPU is active.

6.5 Pins Sample Configuration

The following pins are sampled during SYSRSTn de-assertion:

- Internal pull up/down resistors set the default mode (see Section 1.3, Internal Pull-up and Pull-down Pins, on page 38).
- Higher value, external pull up/down resistors are required to change the default mode of operation.

These signals must remain pulled up or down until SYSRSTn de-assertion (zero hold time in respect to SYSRSTn de-assertion).

Note

- If external logic is used instead of pull-up and pull-down resistors, the logic must drive all of these signals to the desired values during SYSRSTn assertion. To prevent bus contention on these pins, the external logic must float the bus no later than the third TCLK cycle after SYSRSTn de-assertion.
- All reset sampled values are registered in the Sample at Reset register (see the MPP Registers in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*). This is useful for board debug purposes and identification of board and system settings for the host software.
- If a signal is pulled up on the board, it must be pulled to proper voltage level. Certain reset configuration pins are powered by VDD_GE. That pin has multiple voltage options (see Table 32, Recommended Operating Conditions, on page 61).

In each row of Table 28, the order of the pins is from MSb to LSb (e.g., for in the row CPU/DDR/L2 Cache Clocks Select, MPP[2] is the MSB and MPP[10] is the LSB).

Table 28: Reset Configuration

Pin	Configuration Function
MPP[1]	TWSI Serial ROM Initialization
	0 = Disabled 1 = Enabled **NOTE:** Internally pulled down to 0x0. When this pin is set to 0x1, MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively (see Section 4.1, Multi-Purpose Pins Functional Summary, on page 41).
MPP[2],MPP[5], MPP[7]	CPU/DDR/L2 Cache Clocks Select
	0x0-0x4 = Reserved 0x5 = CPU clock: 600 MHz, DDR clock: 200 MHz, L2 cache clock: 300 MHz 0x6 = CPU clock: 800 MHz, DDR clock: 200 MHz, L2 cache clock: 400 MHz 0x7 = Reserved **NOTE:** Internally pulled to 0x3.

Table 28: Reset Configuration (Continued)

Pin	Configuration Function
MPP[10], GE_TXD[1:0]	Boot Device
	0x0 = Reserved 0x1 = Boot from SPI flash (SPI_CSn on MPP[0]) 0x2 = Boot from the PCI Express port 0x3 = Reserved 0x4 = Reserved 0x5 = Boot from NAND flash 0x6 = Reserved 0x7 = Reserved **NOTE:** • Internally pulled to 0x0. • Only SPI signals configured on pins MPP[3:0], can be used for booting from SPI. SPI signals that are multiplexed on other MPPs can only be used after booting (see Section 4.1, Multi-Purpose Pins Functional Summary, on page 41). • When MPP[10], GE_TXD[1:0] is set to 0x1, MPP[3:0] wake up as SPI signals. • When GE_TXD[2:0] is set to 0x5, MPP[5:0] and MPP[19:18] wake up as NAND Flash signals. • For a more detailed description of the bootROM, see the BootROM section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*. • For a more detailed description of the boot from SPI flash or NAND flash, see the SPI Interface and NAND Flash Interface sections in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*. • There is an option to boot from UART when GE_TXD[2:0] = 0x1, 0x2, or 0x5. For a more detailed description of boot from UART, see the BootROM section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
GE_TXD[2]	PCI Express Clock (100 MHz Differential Clock) Configuration
	0x0 = The device uses an external source for PCI Express clock. Pins PEX_CLK_P/PEX_CLK_N are inputs. 0x1 = The device uses an internally generated clock for PCI Express clock. Pins PEX_CLK_P/PEX_CLK_N are outputs, driving out the PCI Express differential clock. **NOTE:** Internally pulled to 0x1.
GE_TXD[3]	SSCG Disable
	0 = Enable 1 = Disable **NOTE:** Internally pulled to 0x1.
GE_MDC	Reserved
	Must be 0x1 during reset. Either leave the signal floating (internally pulled up to 0x1) or pull the signal to 0x1 during reset.
GE_TXCTL	Used for internal testing
	Must be 0x0 during reset. Either leave the signal floating (internally pulled down to 0x0) or pull the signal to 0x0 during reset.

Table 28: Reset Configuration (Continued)

Pin	Configuration Function
MPP[3]	Used for internal testing
	Must be 0x0 during reset. Either leave the signal floating or pull the signal to 0x0 during reset. **NOTE:** Internally pulled to 0x0.

6.6 Serial ROM Initialization

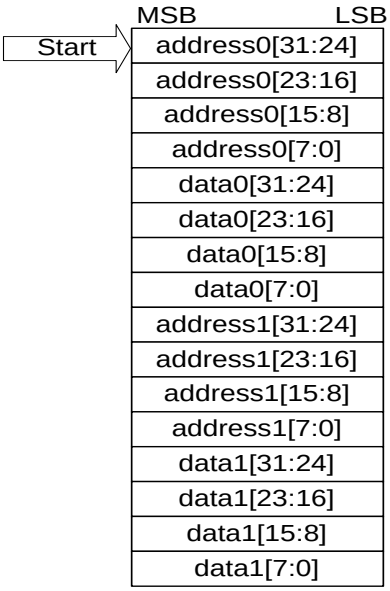
The device supports initialization of ALL of its internal and configuration registers through the TWSI master interface. If serial ROM initialization is enabled, the device TWSI master starts reading initialization data from serial ROM and writes it to the appropriate registers, upon de-assertion of SYSRSTn.

When using Serial ROM Initialization, the MPP[9:8] pins must be configured to as TW_SCK (MPP[9]) and TW_SDA (MPP[8]).

6.6.1 Serial ROM Data Structure

Serial ROM data structure consists of a sequence of 32-bit address and 32-bit data pairs, as shown in Figure 3.

Figure 3: Serial ROM Data Structure



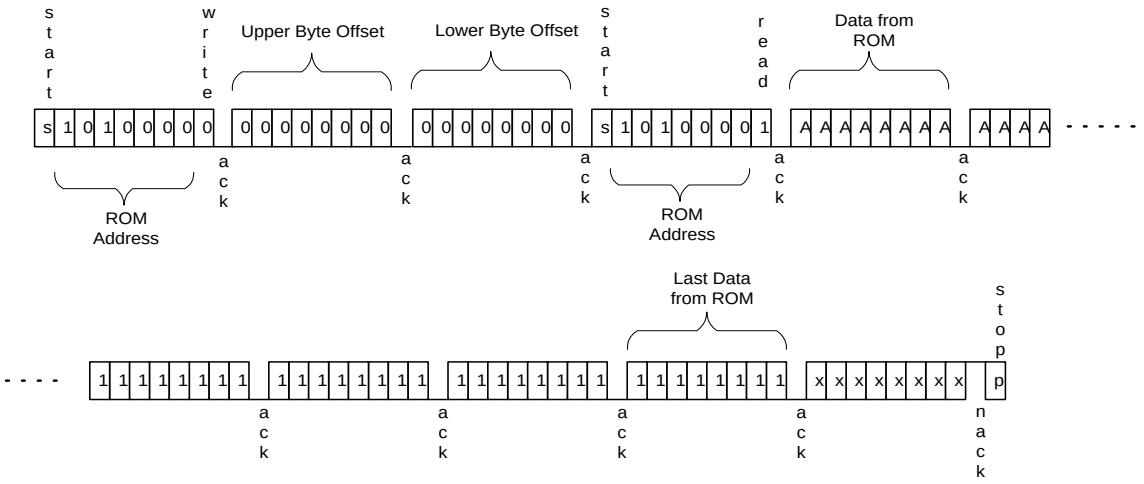
The serial ROM initialization logic reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on address decoding result, writes the next four bytes to the required target.

The Serial Initialization Last Data Register contains the expected value of last serial data item (default value is 0xFFFFFFFF). When the device reaches last data, it stops the initialization sequence.

6.6.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the device starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, to set the ROM byte offset to 0x0. Then, it performs the sequence of reads, until it reaches last data item, as shown in Figure 4.

Figure 4: Serial ROM Read Example



For a detailed description of TWSI implementation, see the Two-Wire Serial Interface section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

- Initialization data must be programmed in the serial ROM starting at offset 0x0.
- The device assumes 7-bit serial ROM address of ‘b1010000.
- After receiving the last data identifier (default value is 0xFFFFFFFF), the device receives an additional byte of dummy data. It responds with no-ack and then asserts the stop bit.
- The serial EEPROM must contain two address offset bytes (It must not be less than a 256 byte ROM.).

6.7 Boot Sequence

The device requires that SYSRSTn stay asserted for at least 300 µs after power and clocks are stable. The following procedure describes the boot sequence starting with the reset assertion:

1. While SYSRSTn is asserted, the CPU PLL and the core PLL are locked.
2. Upon SYSRSTn de-assertion, the pad drive auto-calibration process starts. It takes 512 TCLK cycles.
3. If Serial ROM initialization is enabled, an initialization sequence is started.
4. If configured to boot from NAND flash (and BootROM is disabled), the device also performs a NAND Flash boot sequence to prepare page 0 in the NAND flash device for read.

Upon completing the above sequence, the internal CPU reset is de-asserted, and the CPU starts executing boot code from the boot device (SPI flash, NAND flash, or internal Boot ROM), according to sample at reset setting, see Table 28, Reset Configuration, on page 52.

For bootROM details, see the BootROM section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.

As part of the CPU boot code, the CPU typically performs the following:

- Configures the PCI Express address map.
- Configures the proper SDRAM controller parameters, and then triggers SDRAM initialization (sets <InitEn> bit [0] to 1 in the SDRAM Initialization Control register).
- Sets the <PEXEn> bits in the CPU Control and Status register to wake up the PCI Express link.

7 JTAG Interface

To enable board testing, the device supports a test mode operation through its JTAG boundary scan interface.

The JTAG interface is IEEE 1149.1 standard compliant. It supports mandatory and optional boundary scan instructions.

7.1 TAP Controller

The Test Access Port (TAP) is constructed with a 5-pin interface and a 16-state Finite State Machine (FSM), as defined by IEEE JTAG standard 1149.1.

To place the device in a functional mode, reset the JTAG state machine to disable the JTAG interface.

According to the IEEE 1149.1 standard, the JTAG state machine is not reset when the 88F6180 SYSRSTn is asserted. The JTAG state machine can only be reset by one of the following methods:

- Asserting JT_RSTn.
- Setting JT_TMS_CORE for at least five JT_CLK cycles.

To place the device in one of the boundary scan test mode, the JTAG state machine must be moved to its control states. JT_TMS_CORE and JT_TDI inputs control the state transitions of the JTAG state machine, as specified in the IEEE 1149.1 standard. The JTAG state machine will shift instructions into the Instruction register while in *SHIFT-IR* state and shift data into and from the various data registers when in *SHIFT-DR* state.

7.2 Instruction Register

The Instruction register (IR) is a 4-bit, two-stage register. It contains the command that is shifted in when the TAP FSM is in the *Shift-IR* state. When the TAP FSM is in the *Capture-IR* state, the IR outputs all four bits in parallel.

Table 29 lists the instructions supported by the device.

Table 29: Supported JTAG Instructions

Instruction	Code	Description
HIGHZ	0011	Select the single bit Bypass register between TDI and TDO. Sets the device output pins to high-impedance state.
IDCODE	0010	Selects the Identification register between TDI and TDO. This 32-bit register is used to identify the device.
EXTEST	0000	Selects the Boundary Scan register between TDI and TDO. Outputs the boundary scan register cells to drive the output pins of the device. Inputs the boundary scan register cell to sample the input pin of the device.
SAMPLE/PRELOAD	0001	Selects the Boundary Scan register between TDI and TDO. Samples input pins of the device to input boundary scan register cells. Preloads the output boundary scan register cells with the Boundary Scan register value.
BYPASS	1111	Selects the single bit Bypass register between TDI and TDO. This allows for rapid data movement through an untested device.

7.3 Bypass Register

The Bypass register (BR) is a single bit serial shift register that connects TDI to TDO, when the IR holds the Bypass command, and the TAP FSM is in *Shift-DR* state. Data that is driven on the TDI input pin is shifted out one cycle later on the TDO output pin. The Bypass register is loaded with 0 when the TAP FSM is in the *Capture-DR* state.

7.4 JTAG Scan Chain

The JTAG Scan Chain is a serial shift register used to sample and drive all of the device pins during the JTAG tests. It is a 2-bit per pin shift register in the device, thereby allowing the shift register to sequentially access all of the data pins both for driving and strobing data. For further details, refer to the BSDL Description file for the device.

7.5 ID Register

The ID register is a 32-bit deep serial shift register. The ID register is loaded with vendor and device information when the TAP FSM is in the *Capture-DR* state. The Identification code format of the ID register is shown in Table 30, which describes the various ID Code fields.

Table 30: IDCODE Register Map

Bits	Value	Description
31:28	0x0	Version (4'b0010 for version A0, 4'b0011 for A1, etc.)
27:12	0x6180	Part number
11:1	0x1AB	Manufacturer ID
0	1	Mandatory

8 Electrical Specifications (Preliminary)

Note The numbers specified in this section are PRELIMINARY and SUBJECT TO CHANGE.

8.1 Absolute Maximum Ratings

Table 31: Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD	-0.5	1.2	V	Core and CPU voltage
CPU_PLL_AVDD CORE_PLL_AVDD	-0.5	2.2	V	Analog supply for the internal PLL
SSCG_AVDD	-0.5	2.2	V	Analog supply for: Internal Spread Spectrum Clock Generator
VDD_GE	-0.5	4.0	V	I/O voltage for: RGMII/MII/MMII/SMI interface
VDD_M	-0.5	2.2	V	I/O voltage for: SDRAM interface
VDDO	-0.5	4.0	V	I/O voltage for: MPP, TWSI, JTAG, SDIO, I^2S, and SPI, interfaces
VHV	-0.5	3.0	V	I/O voltage for eFuse burning
PEX_AVDD	-0.5	2.2	V	Analog supply for: PCI Express interface
USB_AVDD	-0.5	4.0	V	Analog supply for: USB interface
XTAL_AVDD	-0.5	2.2	V	Analog supply for internal clock inverter for crystal support and current source for USB PHYs
RTC_AVDD	-0.5	2.2	V	Analog supply for: RTC interface
T_C	-40	125	° C	Case temperature
T_{STG}	-40	125	° C	Storage temperature

Caution

- Exposure to conditions at or beyond the maximum rating may damage the device.
- Operation beyond the recommended operating conditions (Table 32) is neither recommended nor guaranteed.

8.2 Recommended Operating Conditions

Table 32: Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
VDD	0.95	1.0	1.05	V	Core and CPU voltage
CPU_PLL_AVDD CORE_PLL_AVDD	1.7	1.8	1.9	V	Analog supply for the internal PLL
SSCG_AVDD	1.7	1.8	1.9	V	Analog supply for: Internal Spread Spectrum Clock Generator
VDD_GE	3.15	3.3	3.45	V	I/O voltage for: RGMII/MII/MMII/SMI interfaces
	1.7	1.8	1.9	V	I/O voltage for: RGMII/SMI interfaces
VDD_M	1.7	1.8	1.9	V	I/O voltage for: SDRAM interface
VDDO	3.15	3.3	3.45	V	I/O voltage for: MPP, TWSI, JTAG, SDIO, I^2S, and SPI, interfaces
VHV (during eFuse Burning mode)	2.375	2.5	2.625	V	I/O voltage for eFuse burning **NOTE:** If the VHV voltage is higher than VDD voltage (burning mode), VDD must be powered before VHV, to prevent the fuse from being accidentally burned.
VHV (during eFuse Reading mode)	0.95	1.0	1.05	V	I/O voltage for eFuse reading **NOTE:** It is recommended that if only a read operation is required, VHV would be connected to the device VDD power.
PEX_AVDD	1.7	1.8	1.9	V	Analog supply for: PCI Express interface
USB_AVDD	3.15	3.3	3.45	V	Analog supply for: USB interface
XTAL_AVDD	1.7	1.8	1.9	V	Analog supply for: Internal clock inverter for crystal support and current source for USB PHYs

Table 32: Recommended Operating Conditions (Continued)

Parameter	Min	Typ	Max	Units	Comments
RTC_AVDD	1.7	1.8	1.9	V	Analog supply for RTC in Regular mode
	1.3	1.5	1.7	V	Analog supply for RTC in Battery Back-up mode
TJ	0		105	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

8.3 Thermal Power Dissipation

Note Before designing a system, Marvell recommends reading application note *AN-63: Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

The purpose of the Thermal Power Dissipation table is to support system engineering in thermal design.

Table 33: Thermal Power Dissipation

Interface	Symbol	Test Conditions	Typ	Units
Core (including CPU)—VDD 1.0V	P_{VDD}	CPU @ 600 MHz, L2 @ 300 MHz, Core @ 166 MHz	930	mW
		CPU @ 800 MHz, L2 @ 400 MHz, Core @ 166 MHz	1000	mW
RGMII 1.8V interface	P_{RGMII}		30	mW
RGMII (10/100 RGMII only) 3.3V interface	P_{RGMII}		50	mW
MII/MMII 3.3V interface	P_{MII}		10	mW
Miscellaneous interfaces (JTAG, TWSI, UART, NAND flash, Audio, SDIO, and SPI)	P_{MISC}		50	mW
DDR2 SDRAM interface (On Board, 16-bit, 200 MHz)	P_{DDR2}	Two on board devices, 75 ohm ODT termination	180	mW
eFuse during Burning mode **NOTE:** Since the eFuse burn is performed only once, there is no thermal effect after the burn has finished.	P_{FUSE}		50	mW
eFuse during Reading mode	P_{FUSE}		25	mW
PCI Express interface	P_{PEX}		100	mW
USB interface	P_{USB}		120	mW

Notes:

1. The values are for nominal voltage.
2. Power in mW is calculated using the typical recommended VDDIO specification for each power rail.

8.4 Current Consumption

The purpose of the Current Consumption table is to support board power design and power module selection.

Table 34: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
Core (including CPU)—VDD 1.0V	I_{VDD}	CPU @ 600 MHz, L2 @ 300 MHz, Core @ 166 MHz	1930	mA
		CPU @ 800 MHz, L2 @ 400@ MHz, Core @ 166 MHz	2000	mA
RGMII 1.8V or 3.3V interface	I_{RGMII}		25	mA
MII/MMII 3.3V interface	I_{MII_MMII}		25	mA
Miscellaneous interfaces (JTAG, TWSI, UART, NAND flash, Audio, SDIO, and SPI)	I_{MISC}		25	mA
DDR2 SDRAM interface (On Board 16-bit 200 MHz)	I_{DDR2}	Two on board devices, 75 ohm ODT termination	450	mA
eFuse during Burning mode	I_{FUSE}		20	mA
eFuse during Reading mode	I_{FUSE}		25	mA
PCI Express interface	I_{PEX}		50	mA
USB interface	I_{USB}		40	mA

Notes:

1. Current in mA is calculated using maximum recommended VDDIO specification for each power rail.
2. All output clocks toggling at their specified rate.
3. Maximum drawn current from the power supply.

8.5 DC Electrical Specifications

Note

See Section 1.3, Internal Pull-up and Pull-down Pins, on page 38 for internal pullup/pulldown information.

8.5.1 General 3.3V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 35 are applicable for the following interfaces and signals:

- JTAG
- RGMII (10/100 Mbps)/MII/MMII
- Secure Digital Input/Output (SDIO)
- S/PDIF / I^2S (Audio)
- NAND flash
- UART
- MPP
- PTP
- SYSRSTn

In the following table, for the JTAG, SDIO, S/PDIF / I^2S, NAND flash, UART, PTP, and MPP interfaces, VDDIO means the VDDO power rail. For the RGMII/MII/MMII interface, VDDIO means the VDD_GE power rail.

Table 35: General 3.3V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.2 RGMII, SMI and REF_CLK_XIN 1.8V (CMOS) DC Electrical Specifications

In the following table, for the RGMII interface, VDDIO means the VDD_GE power rail.

In the following table, for the REF_CLK_XIN pin, VDDIO means the XTAL_AVDD power rail.

Table 36: RGMII 1.8V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.35*VDDIO	V	-
Input high level	VIH		0.65*VDDIO		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.45	V	-
Output high level	VOH	IOH = -2 mA	VDDIO-0.45		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.3 SDRAM DDR2 Interface DC Electrical Specifications

In the following table, VREF is VDD_M/2 and VDDIO means the VDD_M power rail.

Table 37: SDRAM DDR2 Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL	-	-0.3		VREF - 0.125	V	-
Input high level	VIH	-	VREF + 0.125		VDDIO + 0.3	V	-
Output low level	VOL	IOL = 13.4 mA			0.28	V	-
Output high level	VOH	IOH = -13.4 mA	1.42			V	-
Rtt effective impedance value	RTT	See note 2	120	150	180	ohm	1 , 2
			60	75	90	ohm	1 , 2
			40	50	60	ohm	1 , 2
Deviation of VM with respect to VDDQ/2	dVm	See note 3	-6		6	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply VREF +/- 0.25 to input pin separately,
   then measure current I(*VREF* +0.25) and I(*VREF* -0.25) respectively.

$$RTT = \frac{0.5}{I_{(VREF+0.25)} - I_{(VREF-0.25)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1 \right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.4 Two-Wire Serial Interface (TWSI) 3.3V DC Electrical Specifications

In the following table, VDDIO means the VDDO power rail.

Table 38: TWSI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.5.5 Serial Peripheral Interface (SPI) 3.3V DC Electrical Specifications

In the following table VDDIO means the VDDO power rail.

Table 39: SPI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 4 mA	-		0.4	V	-
Output high level	VOH	IOH = -4 mA	VDDIO-0.6		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

8.6 AC Electrical Specifications

See Section 8.7, Differential Interface Electrical Characteristics, on page 92 for differential interface specifications.

8.6.1 Reference Clock AC Timing Specifications

Table 40: Reference Clock AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
CPU and Core Reference Clock					
Frequency	$F_{REF\_CLK\_XIN}$	25 - 50 ppm	25 + 50 ppm	MHz	
Clock duty cycle	$DC_{REF\_CLK\_XIN}$	40	60	%	
Slew rate	$SR_{REF\_CLK\_XIN}$	0.7		V/ns	1
Pk-Pk jitter	$JR_{REF\_CLK\_XIN}$		200	ps	
Ethernet Reference Clock					
Frequency in MII/MMII-MAC mode	$F_{GE\_TXCLK\_OUT}$ F_{GE_RXCLK}	2.5 - 100 ppm	50 + 100 ppm	MHz	
MII/MMII-MAC mode clock duty cycle	$DC_{GE\_TXCLK\_OUT}$ DC_{GE_RXCLK}	35	65	%	
Slew rate	$SR_{GE\_TXCLK\_OUT}$ SR_{GE_RXCLK}	0.7		V/ns	1
Audio External Reference Clock					
Audio external reference clock	F_{AU_EXTCLK}	256 X F_s		kHz	3
S/PDIF Recovered Master Clock					
S/PDIF recovered master clock	$F_{AU\_SPDFRMCLK}$	256 X F_s		kHz	3
I^2S Reference Clock					
I^2S clock	F_{I2S_BCLK}	64 X F_s		kHz	3
SPI Output Clock					
SPI output clock	F_{SPI_SCK}	TCLK/30	TCLK/4	MHz	2
RTC Reference Clock					
RTC_XIN crystal frequency	F_{RTC_XIN}	32.768		kHz	4
SMI Master Mode Reference Clock					
SMI output MDC clock	F_{GE_MDC}	TCLK/128		MHz	
TWSI Master Mode Reference Clock					
SCK output clock	F_{TW_SCK}		TCLK/ 1600	kHz	6
PTP Reference Clock					
Frequency	F_{PTP_CLK}	125 - 100 ppm	125 + 100 ppm	MHz	
Clock duty cycle	DC_{PTP_CLK}	40	60	%	

Table 40: Reference Clock AC Timing Specifications (Continued)

Description	Symbol	Min	Max	Units	Notes
Slew rate	SR_{PTP_CLK}	0.7		V/ns	1
Pk-Pk jitter	JR_{PTP_CLK}		100	ps	

Notes:

1. Slew rate is defined from 20% to 80% of the reference clock signal.
2. For additional information regarding configuring this clock, see the Serial Memory Interface Control Register in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications*.
3. F_S is the audio sample rate, which can be configured to 44.1 kHz, 48 kHz, or 96 kHz (see the Audio (I^2S / S/PDIF) Interface section in the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications).*
4. The RTC design was optimized for a standard CL = 12.5 pF crystal. No passive components are provided internally. Connect the crystal and the passive network as recommended by the crystal manufacturer.
5. For the minimum value refer to the Baud Rate Register section of the *88F6180, 88F6190, 88F6192, and 88F6281 Functional Specifications.*

8.6.2 SDRAM DDR2 Interface AC Timing

8.6.2.1 SDRAM DDR2 Interface AC Timing Table

Table 41: SDRAM DDR2 Interface AC Timing Table

Description	Symbol	200 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	200.00		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.50	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.50	-	ns	-
DQ and DM output pulse width	tDIPW	0.37	-	tCK	-
DQS output high pulse width	tDQSH	0.37	-	tCK	-
DQS output low pulse width	tDQSL	0.37	-	tCK	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK	1
CLK-CLKn rising edge to DQS output rising edge	tDQSS	-0.11	0.11	tCK	-
DQS write preamble	tWPRE	0.35	-	tCK	-
DQS write postamble	tWPST	0.42	-	tCK	-
CLK-CLKn high-level width	tCH	0.45	0.55	tCK	1
CLK-CLKn low-level width	tCL	0.45	0.55	tCK	1
DQ input setup time relative to DQS in transition	tDSI	-0.55	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	1.50	-	ns	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	1.70	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	1.70	-	ns	1, 2
Address and control output pulse width	tIPW	0.67	-	tCK	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

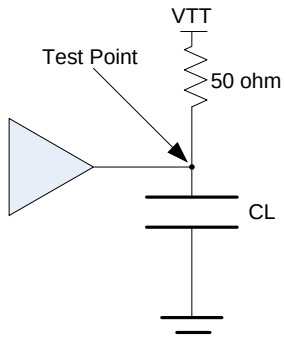
General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 8 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output with CLK-CLKn falling edge.
   For more information, see register settings.

8.6.2.2 SDRAM DDR2 Interface Test Circuit

Figure 5: SDRAM DDR2 Interface Test Circuit



8.6.2.3 SDRAM DDR2 Interface AC Timing Diagrams

Figure 6: SDRAM DDR2 Interface Write AC Timing Diagram

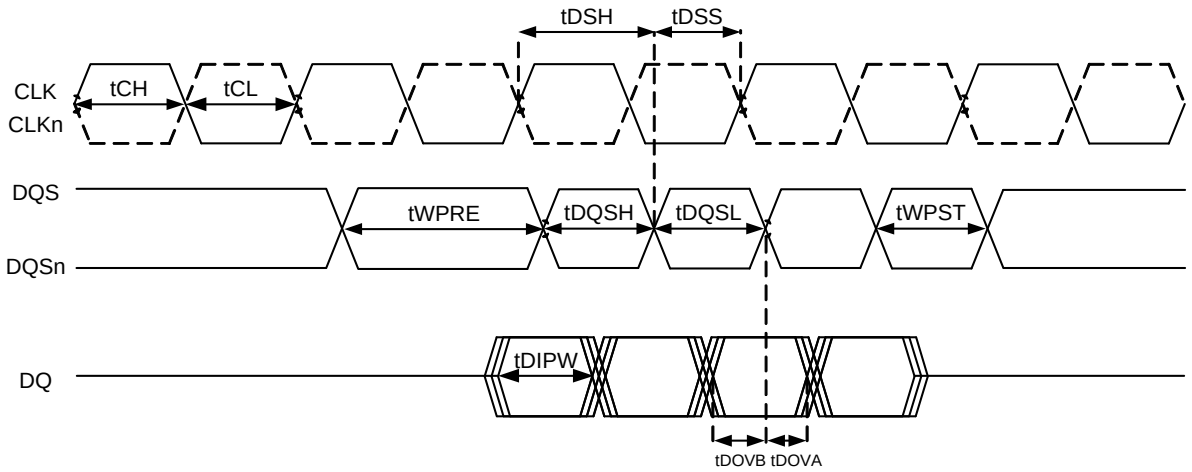


Figure 7: SDRAM DDR2 Interface Address and Control AC Timing Diagram

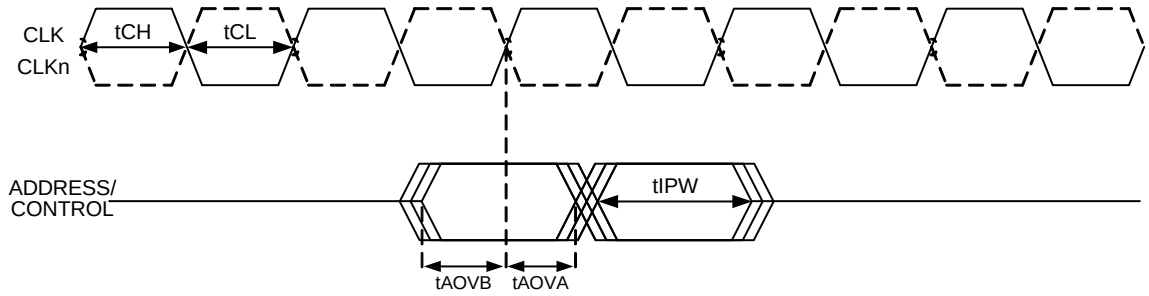
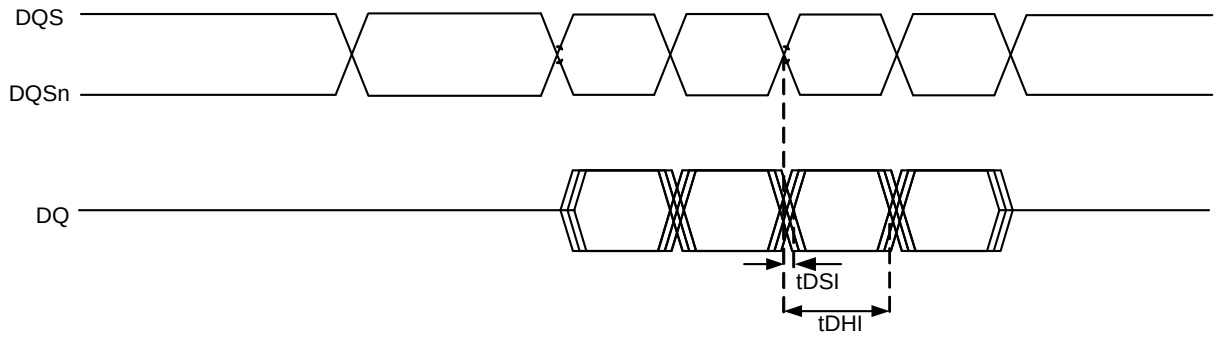


Figure 8: SDRAM DDR2 Interface Read AC Timing Diagram



8.6.3 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

8.6.3.1 RGMII AC Timing Table

Table 42: RGMII 10/100/1000 AC Timing Table at 1.8V

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	125.0		MHz	-
Data to Clock output skew	Tskew T	-0.50	0.50	ns	2
Data to Clock input skew	Tskew R	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

Table 43: RGMII 10/100 AC Timing Table at 3.3V

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	25.0		MHz	-
Data to Clock output skew	Tskew T	-0.50	0.50	ns	2
Data to Clock input skew	Tskew R	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

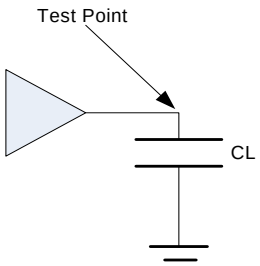
General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

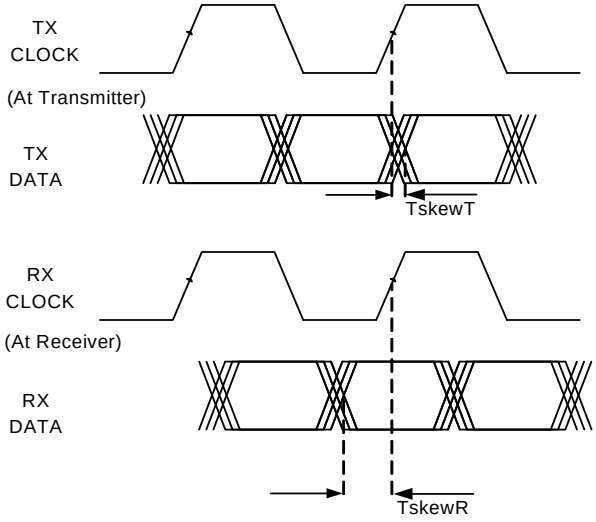
8.6.3.2 RGMII Test Circuit

Figure 9: RGMII Test Circuit



8.6.3.3 RGMII AC Timing Diagram

Figure 10: RGMII AC Timing Diagram



8.6.4 Media Independent Interface/Marvell Media Independent Interface (MII/MMII) AC Timing

8.6.4.1 MII/MMII MAC Mode AC Timing Table

Table 44: MII/MMII MAC Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	3.5	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	2.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	10.0	ns	1

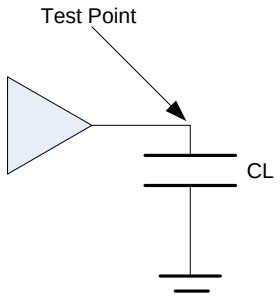
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

8.6.4.2 MII/MMII MAC Mode Test Circuit

Figure 11: MII/MMII MAC Mode Test Circuit



8.6.4.3 MII/MMII MAC Mode AC Timing Diagrams

Figure 12: MII/MMII MAC Mode Output Delay AC Timing Diagram

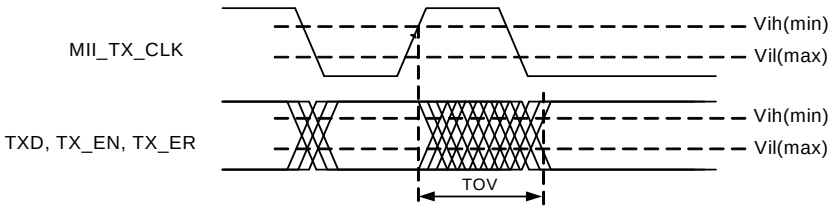
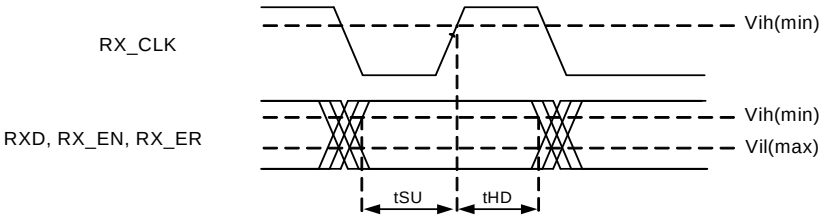


Figure 13: MII/MMII MAC Mode Input AC Timing Diagram



8.6.5 Serial Management Interface (SMI) AC Timing

8.6.5.1 SMI Master Mode AC Timing Table

Table 45: SMI Master Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.4	0.6	tCK	-
MDIO input setup time relative to MDC rise time	tSU	40.0	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.0	-	ns	-
MDIO output valid before MDC rise time	tOVB	15.0	-	ns	1
MDIO output valid after MDC rise time	tOVA	15.0	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For MDC signal, the load is CL = 390 pF, and for MDIO signal, the load is CL = 470 pF.

2. See "Reference Clocks" table for more details.

8.6.5.2 SMI Master Mode Test Circuit

Figure 14: MDIO Master Mode Test Circuit

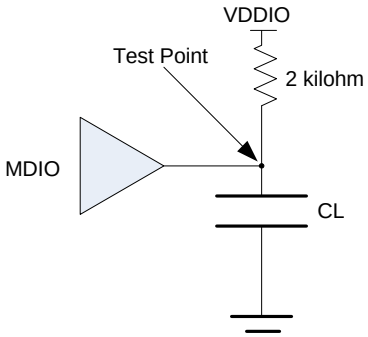
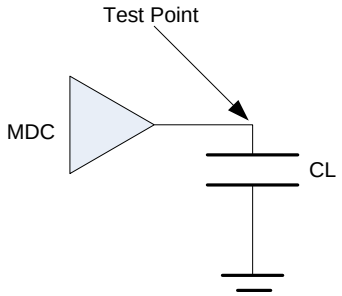


Figure 15: MDC Master Mode Test Circuit



8.6.5.3 SMI Master Mode AC Timing Diagrams

Figure 16: SMI Master Mode Output AC Timing Diagram

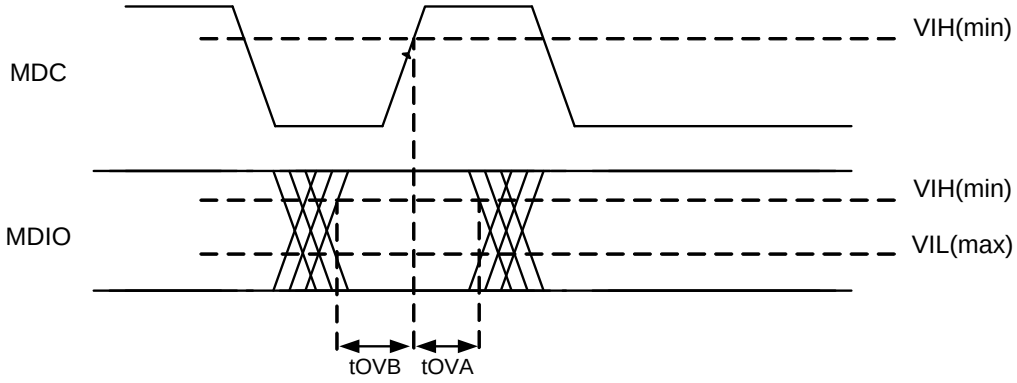
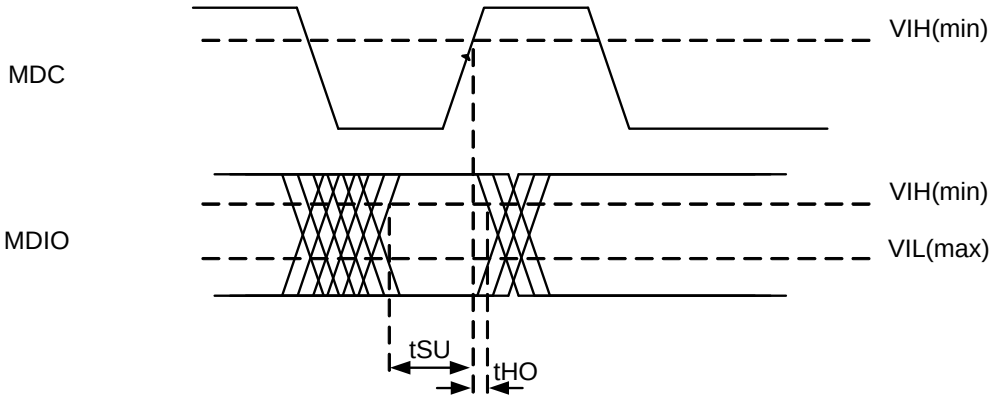


Figure 17: SMI Master Mode Input AC Timing Diagram



8.6.6 JTAG Interface AC Timing

8.6.6.1 JTAG Interface AC Timing Table

Table 46: JTAG Interface AC Timing Table

Description	Symbol	30 MHz		Units	Notes
		Min	Max		
JTClk frequency	fCK	30.0		MHz	-
JTClk minimum pulse width	Tpw	0.45	0.55	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.50	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	6.67	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	13.0	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	8.33	ns	1

Notes:

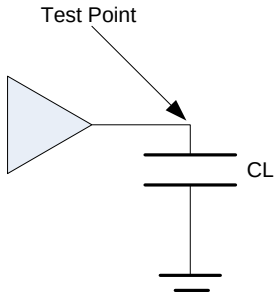
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 10 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.

8.6.6.2 JTAG Interface Test Circuit

Figure 18: JTAG Interface Test Circuit



8.6.6.3 JTAG Interface AC Timing Diagrams

Figure 19: JTAG Interface Output Delay AC Timing Diagram

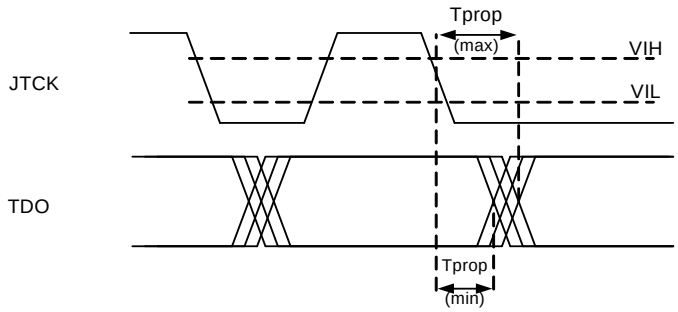
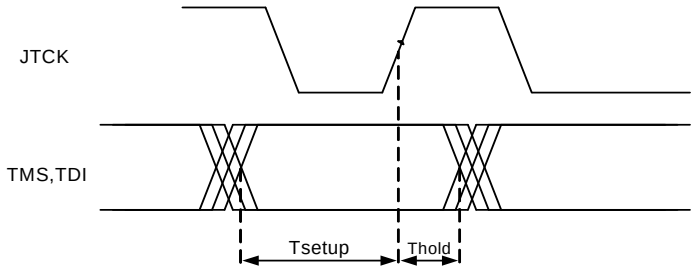


Figure 20: JTAG Interface Input AC Timing Diagram



8.6.7 Two-Wire Serial Interface (TWSI) AC Timing

8.6.7.1 TWSI AC Timing Table

Table 47: TWSI Master AC Timing Table

Description	Symbol	Min	Max	Units	Notes
SCK clock frequency	fCK	See note 1		kHz	1
SCK minimum low level width	tLOW	0.47	-	tCK	2
SCK minimum high level width	tHIGH	0.40	-	tCK	2
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	2, 3
SDA and SCK fall time	tf	-	300.0	ns	2, 3
SDA output delay relative to SCK falling edge	tOV	0.0	0.4	tCK	2

Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
3. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

Table 48: TWSI Slave AC Timing Table

Description	Symbol	100 kHz		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

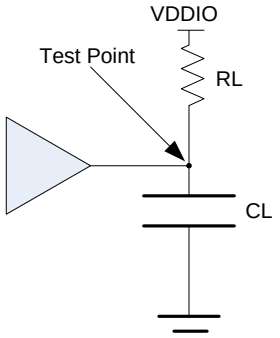
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

8.6.7.2 TWSI Test Circuit

Figure 21: TWSI Test Circuit



8.6.7.3 TWSI AC Timing Diagrams

Figure 22: TWSI Output Delay AC Timing Diagram

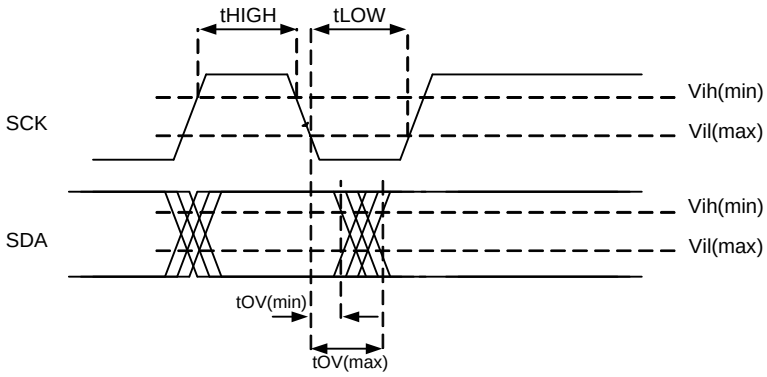
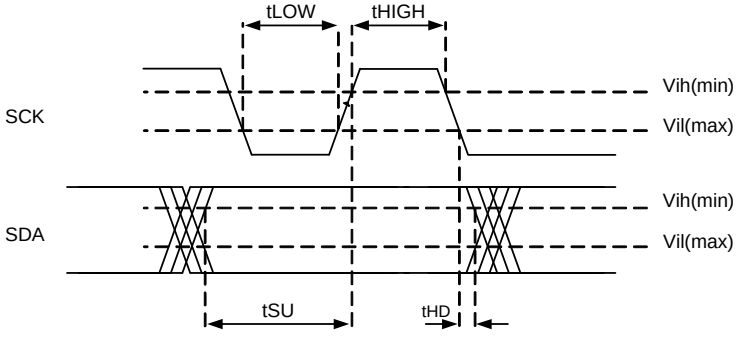


Figure 23: TWSI Input AC Timing Diagram



8.6.8 Sony/Philips Digital Interconnect Format (S/PDIF) AC Timing

8.6.8.1 S/PDIF AC Timing Table

Table 49: S/PDIF AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Output frequency accuracy	Ftxtol	-50.0	50.0	ppm	1
Input frequency accuracy	Frxtol	-100.0	100.0	ppm	-
Output jitter - total peak-to-peak	Txjit	-	0.05	UI	1, 2
Jitter transfer gain	Txjitgain	-	3.0	dB	3
Input jitter - total peak-to-peak	Rxjit	-	10.0	UI	4
		-	0.25	UI	5
		-	0.2	UI	6

Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

General comment: For more information, refer to the Digital Audio Interface - Part 3: Consumer Applications, IEC 60958-3:2003(E), Chapter 7.3, January 2003.

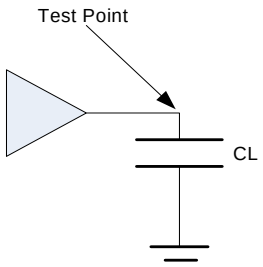
1. For all signals, the load is CL = 10 pF.
2. Using inristic jitter filter.
3. Refer to Figure-8 in IEC 60958-3:2003(E), Chapter 7.3, January 2003.
4. Defined for up to 5 Hz.
5. Defined from 200 Hz to 400 kHz.
6. Defined for above 400 kHz.

Note

For additional information about working with a coax connection, see the *88F6180, 88F6190, 88F6192, and 88F6281 Design Guide*.

8.6.8.2 S/PDIF Test Circuit

Figure 24: S/PDIF Test Circuit



8.6.9 Inter-IC Sound Interface (I^2S) AC Timing

8.6.9.1 Inter-IC Sound (I^2S) AC Timing Table

Table 50: Inter-IC Sound (I^2S) AC Timing Table

Description	Symbol	Min	Max	Units	Notes
I2SBCLK clock frequency	fCK	See note 2		MHz	2
I2SBCLK clock high/low level pulse width	tCH/tCL	0.37	-	tCK	1
I2SDI input setup time relative to I2SBCLK rise time	tSU	0.10	-	tCK	-
I2SDI input hold time relative to I2SBCLK rise time	tHO	0.00	-	ns	-
I2SDO, I2SLRCLK output delay relative to I2SBCLK rise time	tOD	0.10	0.70	tCK	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

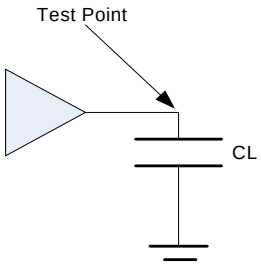
General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 15 pF.

2. See "Reference Clocks" table for more details.

8.6.9.2 Inter-IC Sound (I^2S) Test Circuit

Figure 25: Inter-IC Sound (I^2S) Test Circuit



8.6.9.3 Inter-IC Sound (I^2S) AC Timing Diagrams

Figure 26: Inter-IC Sound (I^2S) Output Delay AC Timing Diagram

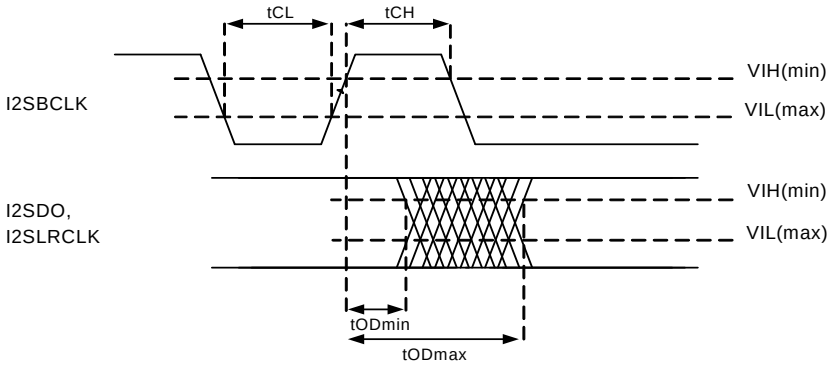
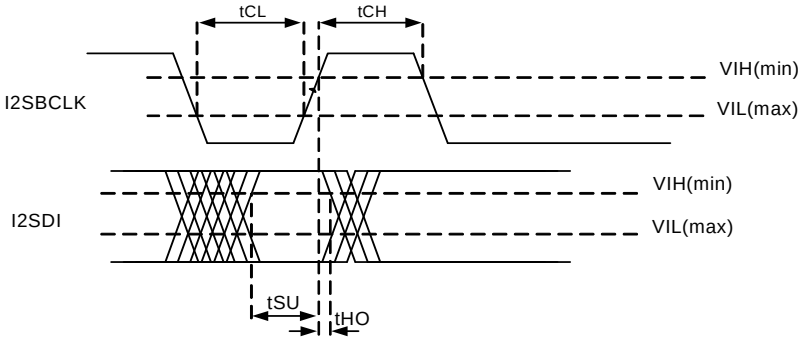


Figure 27: Inter-IC Sound (I^2S) Input AC Timing Diagram



8.6.10 Serial Peripheral Interface (SPI) AC Timing

8.6.10.1 SPI (Master Mode) AC Timing Table

Table 51: SPI (Master Mode) AC Timing Table

Description	Symbol	SPI		Units	Notes
		Min	Max		
SCLK clock frequency	fCK	See Note 3		MHz	3
SCLK high time	tCH	0.46	-	tCK	1
SCLK low time	tCL	0.46	-	tCK	1
SCLK slew rate	tSR	0.5	-	V/ns	1
Data out valid relative to SCLK falling edge	tDOV	-2.5	2.5	ns	1
CS active before SCLK rising edge	tCSB	8.0	-	ns	1
CS not active after SCLK rising edge	tCSA	8.0	-	ns	1
Data in setup time relative to SCLK rising edge	tSU	0.2	-	tCK	2
Data in hold time relative to SCLK rising edge	tHD	5.0	-	ns	2

Notes:

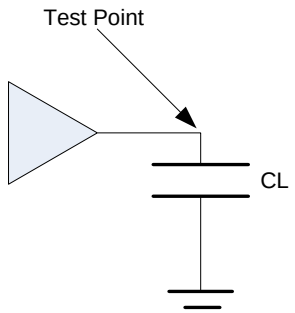
General comment: All values were measured from 0.3*vddio to 0.7*vddio, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. Defined from vddio/2 to vddio/2.
3. See "Reference Clocks" table for more details.

8.6.10.2 SPI (Master Mode) Test Circuit

Figure 28: SPI (Master Mode) Test Circuit



8.6.10.3 SPI (Master Mode) Timing Diagrams

Figure 29: SPI (Master Mode) Output AC Timing Diagram

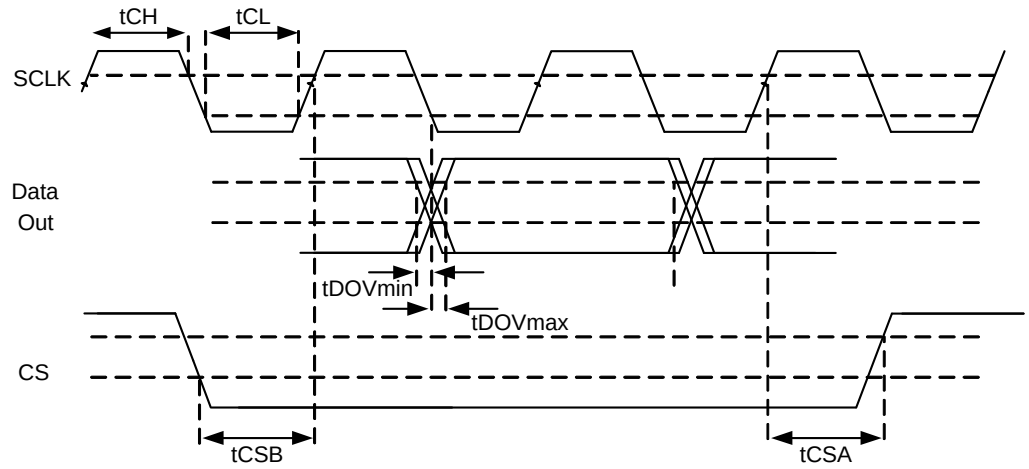
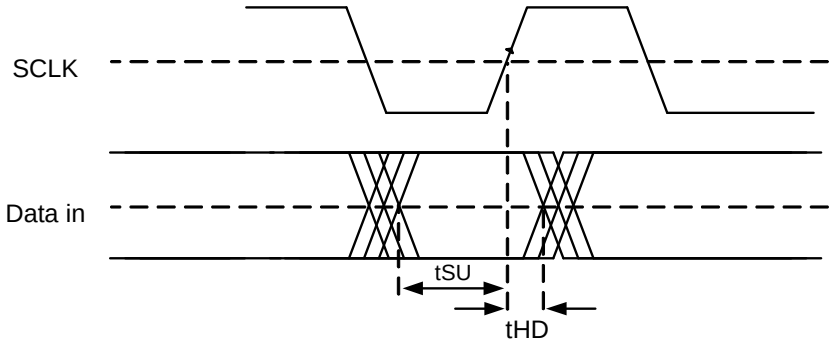


Figure 30: SPI (Master Mode) Input AC Timing Diagram



8.6.11 Secure Digital Input/Output (SDIO) Interface AC Timing

8.6.11.1 Secure Digital Input/Output (SDIO) AC Timing Table

Table 52: SDIO Host in High Speed Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	50	MHz	-
Clock high/low level pulse width	tWL/tWH	0.35	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	3.0	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	6.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	2.5	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	7.0	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2

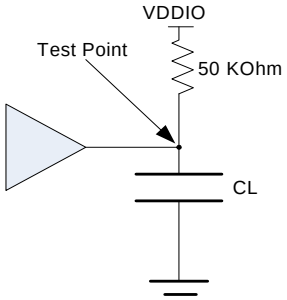
Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD & DAT signals.
3. For all signals, the load is CL = 10 pF.

8.6.11.2 Secure Digital Input/Output (SDIO) Test Circuit

Figure 31: Secure Digital Input/Output (SDIO) Test Circuit



8.6.11.3 Secure Digital Input/Output (SDIO) AC Timing Diagrams

Figure 32: SDIO Host in High Speed Mode Output AC Timing Diagram

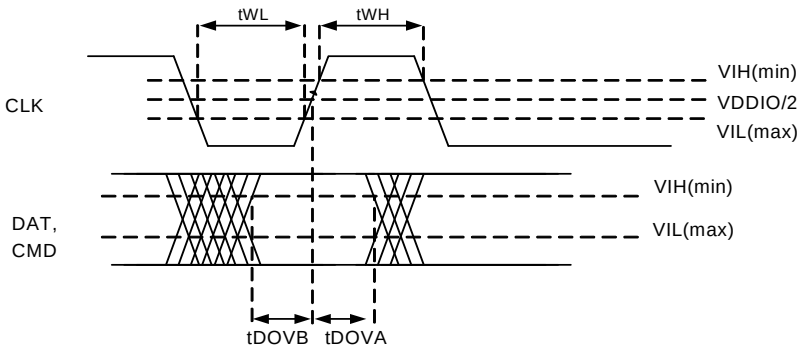
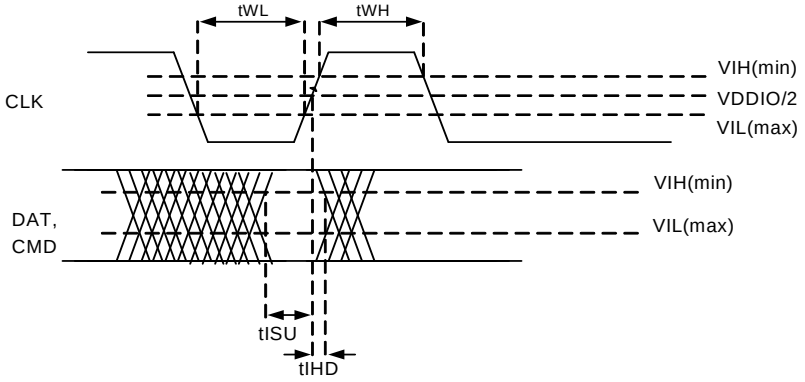


Figure 33: SDIO Host in High Speed Mode Input AC Timing Diagram



8.7 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the following differential interfaces:

- PCI Express Interface Electrical Characteristics
- USB Electrical Characteristics

8.7.1 Differential Interface Reference Clock Characteristics

8.7.1.1 PCI Express Interface Differential Reference Clock Characteristics

Table 53: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	100.0		MHz	-
Clock duty cycle	DCrefclk	0.4	0.6	tCK	-
Differential rising/falling slew rate	SRrefclk	0.6	4.0	V/nS	3
Differential high voltage	VIHrefclk	150.0	-	mV	-
Differential low voltage	VILrefclk	-	-150.0	mV	-
Absolute crossing point voltage	Vcross	250.0	550.0	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140.0	mV	1
Average differential clock period accuracy	Tperavg	-300.0	2800.0	ppm	-
Absolute differential clock period	Tperabs	9.8	10.2	nS	2
Differential clock cycle-to-cycle jitter	Tccjit	-	150.0	pS	-

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 1.1, March 2005, section 2.1.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.
3. Defined from -150 mV to +150 mV on the differential waveform.

PCI Express Interface Spread Spectrum Requirements

Table 54: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	0.0	33.0	kHz	1
Fspread	-0.5	0.0	%	1

Notes:
1. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.

8.7.2 PCI Express Interface Electrical Characteristics

8.7.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 55: PCI Express Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400.0		ps	-
Baud rate tolerance	Bppm	-300.0	300.0	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss	TRLdiff	10.0	-	dB	1
Common mode return loss	TRLcm	6.0	-	dB	1
DC differential TX impedance	ZTXdiff	80.0	120.0	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	10.0	-	dB	1
Common mode return loss	RRLcm	6.0	-	dB	1
DC differential RX impedance	ZRXdiff	80.0	120.0	Ohm	-
DC common input impedance	ZRXcm	40.0	60.0	Ohm	-

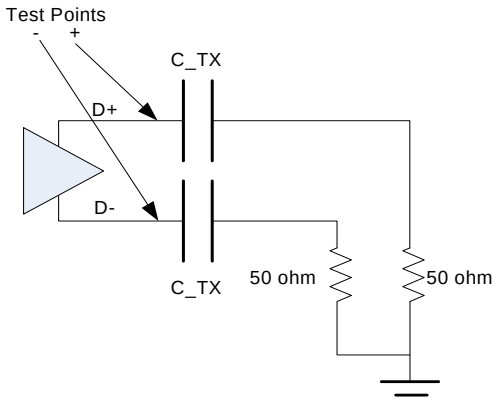
Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.1, March, 2005.

1. Defined from 50 MHz to 1.25 GHz.
2. Does not account for SSC dictated variations.

8.7.2.2 PCI Express Interface Test Circuit

Figure 34: PCI Express Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

8.7.3 USB Electrical Characteristics

8.7.3.1 USB Driver and Receiver Characteristics

Table 56: USB Low Speed Driver and Receiver Characteristics

Description	Symbol	Low Speed		Units	Notes
		Min	Max		
Baud Rate	BR	1.5		Mbps	-
Baud rate tolerance	Bppm	-15000.0	15000.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	3
Data fall time	TLR	75.0	300.0	ns	3, 4
Data rise time	TLF	75.0	300.0	ns	3, 4
Rise and fall time matching	TLRFM	80.0	125.0	%	-
Source jitter total: to next transition	TUDJ1	-95.0	95.0	ns	5
Source jitter total: for paired transitions	TUDJ2	-150.0	150.0	ns	5
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.

Table 57: USB Full Speed Driver and Receiver Characteristics

Description	Symbol	Full Speed		Units	Notes
		Min	Max		
Baud Rate	BR	12.0		Mbps	-
Baud rate tolerance	Bppm	-2500.0	2500.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	4
Output rise time	TFR	4.0	20.0	ns	3, 4
Output fall time	TFL	4.0	20.0	ns	3, 4
Source jitter total: to next transition	TDJ1	-3.5	3.5	ns	5, 6
Source jitter total: for paired transitions	TDJ2	-4.0	4.0	ns	5, 6
Source jitter for differential transition to SE0 transition	TFDEOP	-2.0	5.0	ns	6
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-
Receiver jitter : to next transition	tJR1	-18.5	18.5	ns	6
Receiver jitter: for paired transitions	tJR2	-9.0	9.0	ns	6

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1.. Defined with 1.425 kilohm pull-up resistor to 3.6V.

2.. Defined with 14.25 kilohm pull-down resistor to ground.

3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.

4. See "Data Signal Rise and Fall Time" waveform.

5. Including frequency tolerance. Timing difference between the differential data signals.

6. Defined at crossover point of differential data signals.

Table 58: USB High Speed Driver and Receiver Characteristics

Description	Symbol	High Speed		Units	Notes
		Min	Max		
Baud Rate	BR	480.0		Mbps	-
Baud rate tolerance	Bppm	-500.0	500.0	ppm	-
Driver Parameters					
Data signaling high	VHSOH	360.0	440.0	mV	-
Data signaling low	VHSOL	-10.0	10.0	mV	-
Data rise time	THSR	500.0	-	ps	1
Data fall time	THSF	500.0	-	ps	1
Data source jitter		See note 2			2
Receiver Parameters					
Differential input signaling levels		See note 3			3
Data signaling common mode voltage range	VHSCM	-50.0	500.0	mV	-
Receiver jitter tolerance		See note 3			3

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

8.7.3.2 USB Interface Driver Waveforms

Figure 35: Low/Full Speed Data Signal Rise and Fall Time

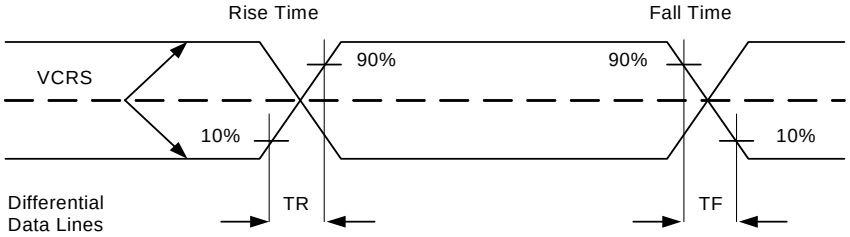


Figure 36: High Speed TX Eye Diagram Pattern Template

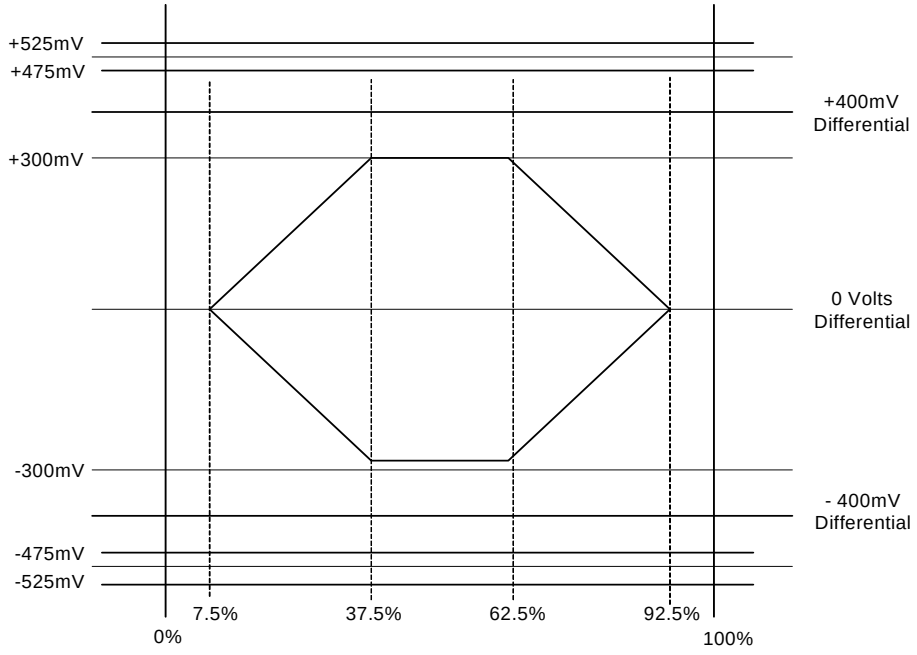
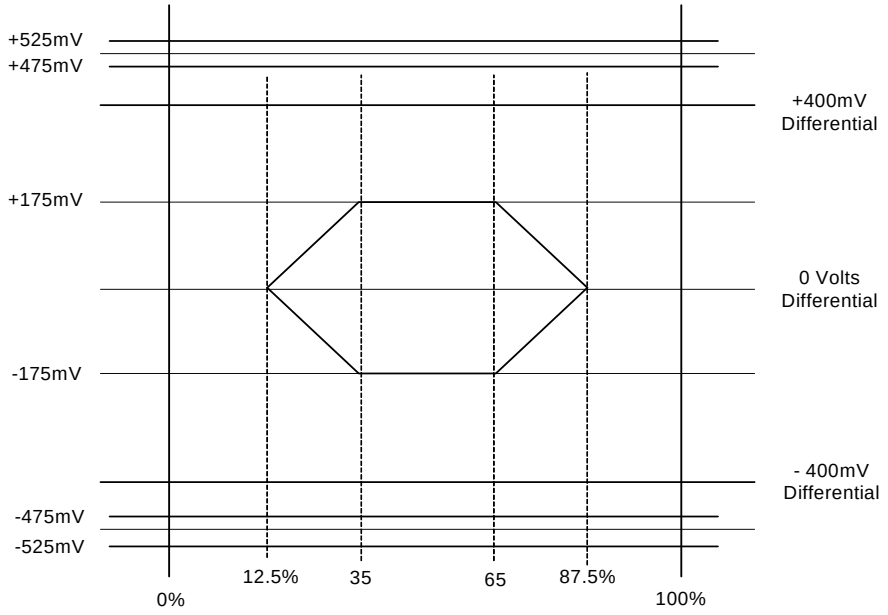


Figure 37: High Speed RX Eye Diagram Pattern Template



9 Thermal Data (Preliminary)

Table 59 provides the package thermal data for the device. This data is derived from simulations that were run according to the JEDEC standard.

Note The thermal parameters are preliminary and subject to change.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products. Before designing a system it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products,* Document Number MV-S300281-00
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Document Number MV-S700019-00.

Table 59: Thermal Data for the 88F6180 in the 225-pin LFBGA Package (Preliminary)

Symbol	Definition	Airflow Value (C/W)		
		0[m/s]	1[m/s]	2[m/s]
θ_{JA}	Thermal resistance: junction to ambient.	27.8	25.4	24.7
Ψ_{JT}	Thermal characterization parameter: junction to case center.	3.2	3.4	3.5
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	10.7		
Ψ_{JB}	Thermal characterization parameter: junction to the bottom of the package.	15.8	15.7	15.6
θ_{JB}	Thermal resistance: junction to the bottom of the package (not air-flow dependent)	15.9		

10 Package

This section provides the 88F6180 package drawing and dimensions.

Figure 38: LFBGA 225-pin Package and Dimensions

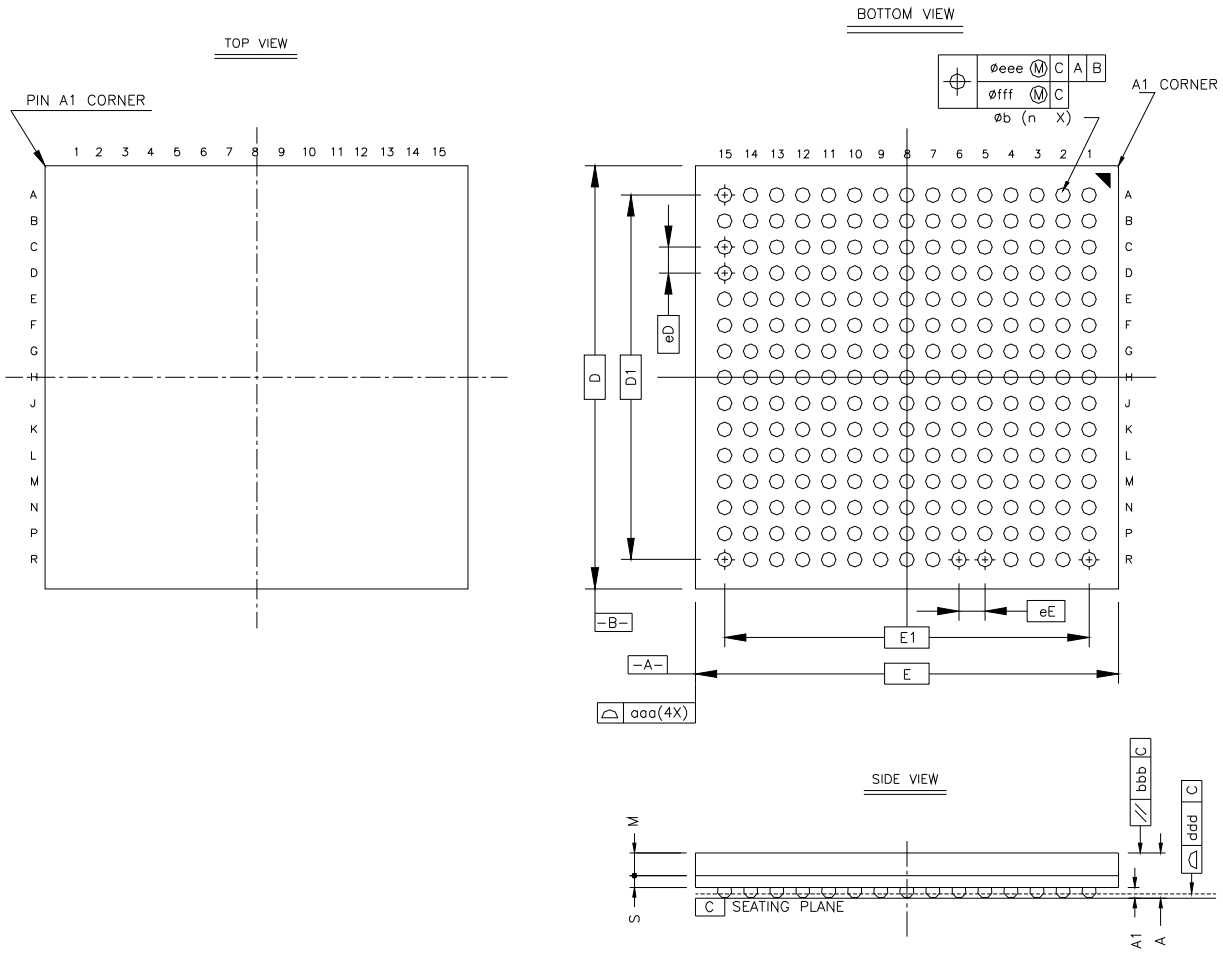


Table 60: LFBGA 225-pin Package Dimensions

		Symbol	Common Dimension (in millimeters)
Package			LFBGA
Body size	X	E	13.000
	Y	D	13.000
Ball pitch	X	eE	0.800
	Y	eD	0.800
Total thickness		A	1.700 maximum
Mold thickness		A3	0.700 ref
Substrate thickness		A2	0.360 ref
Ball diameter			0.450
Standoff		A1	0.250 ~ 0.400
Ball width		b	0.400 ~ 0.500
Package edge tolerance		aaa	0.150
Mold flatness		bbb	0.200
Copolarity		ddd	0.150
Ball offset (package)		eee	0.150
Ball offset (ball)		fff	0.080
Ball count		n	225
Edge ball center-to-center	X	E1	11.200
	Y	D1	11.200

11 Part Order Numbering/Package Marking

11.1 Part Order Numbering

Figure 39 shows the part order numbering scheme for the 88F6180. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 39: Sample Part Number

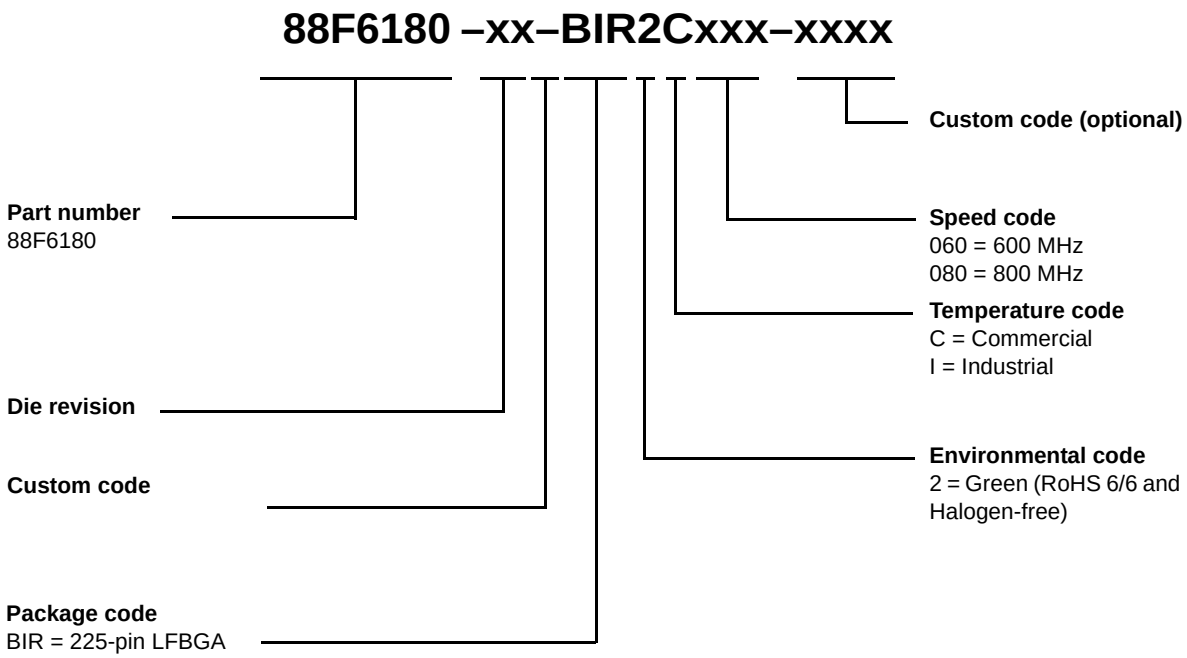


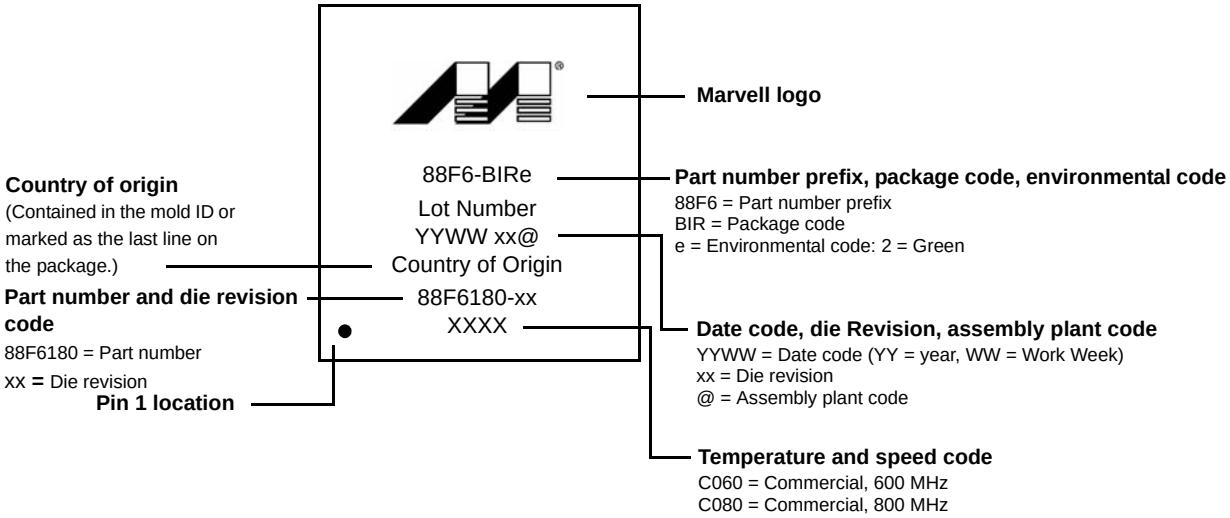
Table 61: Part Order Options

Package Type	Part Order Number
225-pin LFBGA	88F6180-xx-BIR2C060 (Green, RoHS 6/6 and Halogen-free package), 600 MHz
225-pin LFBGA	88F6180-xx-BIR2C080 (Green, RoHS 6/6 and Halogen-free package), 800 MHz

11.2 Package Marking

Figure 40 shows a sample Commercial package marking and pin 1 location for the 88F6180.

Figure 40: Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 62: Revision History

Revision	Date	Comments
E	December 2, 2008	Revision
1. In Figure 1, 88F6180 Pin Logic Diagram, on page 16, changed the GE_TXCLKOUT pin to input/output and added a note under the figure, stating that the pin is an input when used the MII/MMII Transmit Clock.		
2. In Table 3, Power Pin Assignments, on page 19, revised the description of the VDD_GE pin.		
3. In Table 4, Miscellaneous Pin Assignments, on page 20, revised the description of the ISET pin.		
4. In Table 6, PCI Express Interface Pin Assignments, on page 23, revised the description of the PEX_CLK_P/N pins to state that they can be configured as input or output according to the reset strap.		
5. In Table 7, Gigabit Ethernet Port Interface Pin Assignments, on page 24, added a description of the MII/MMII Transmit Clock to the description of the GE_TXCLKOUT pin.		
6. In Table 11, RTC Interface Pin Assignments, on page 29, changed the type for RTC_XOUT to analog.		
7. In the description of signal AU_SPDFRMCLK in Table 16, Audio (S/PDIF / I^2S) Interface Signal Assignment, on page 34, added a reference to the new AU_SPDFRMCLK information in the Reference Clock AC Timing Specifications table.		
8. In Table 21, Unused Interface Strapping, on page 39, revise the description for configuring the PCI Express clock signals.		
9. At the end of Gigabit Ethernet (GbE) Pins Multiplexing on MPP, added a note stating that all relevant Gigabit Ethernet signals must be implemented.		
10. In Table 32, Recommended Operating Conditions, on page 61, for parameter RTC_AVDD Analog supply for RTC in Battery Back-up mode, revised the values for the minimum to 1.3V from 1.4V and for the maximum to 1.7V from 1.6V.		
11. In Table 33, Thermal Power Dissipation, on page 63, for the eFuse during Burning mode parameter added a note: The eFuse burn is done once, and there should be no thermal effect, after it has been burned.		
12. In Table 40, Reference Clock AC Timing Specifications, on page 69: • Revised the names of the Ethernet transmit symbols to $F_{GE\_TXCLK\_OUT}$, $DC_{GE\_TXCLK\_OUT}$, and $SR_{GE\_TXCLK\_OUT}$. • Added the S/PDIF Recovered Master Clock. • For the PTP reference clock, revised the values for the Frequency, Duty Cycle, and Pk-Pk jitter parameters.		
D	October 5, 2008	Revision
1. In Table 6, PCI Express Interface Pin Assignments, on page 23, revised the note in the description of the PEX_CLK_P/N pins.		
2. In Table 20, Internal Pull-up and Pull-down Pins, on page 38, revised the pin number for MRn from G04 to G03.		
3. In Table 21, Unused Interface Strapping, on page 39, added the eFuse strapping.		
4. Revised the attached excel pin map and pin list. See the revision history in the excel file for a list of the pin changes.		
5. In Section 6.1.1, Power-Up Sequence Requirements, on page 48 and Section 6.1.2, Power-Down Sequence Requirements, on page 49, added a power up/down requirements for when VHV is in eFuse Burning mode.		
6. In Table 32, Recommended Operating Conditions, on page 61: • For VHV, revised the two parameters to *VHV (during eFuse Burning mode)* and *VHV (during eFuse Reading mode)* and added notes in the comments column for both VHV voltages. • For VDD_M, PEX_AVDD, and USB_AVDD, revised the comments column. • for RTC_AVDD, revised the values for minimum to 1.4V from 1.3V and for maximum to 1.6V from 1.7V.		
7. In Table 33, Thermal Power Dissipation, on page 63, revised the row for the SDRAM and added a row for the eFuse.		

Table 62: Revision History (Continued)

Revision	Date	Comments
		8. In Table 34, Current Consumption, on page 64, revised the row for the SDRAM and added a row for the eFuse. 9. In Table 40, Reference Clock AC Timing Specifications, on page 69: • For the CPU and Core Reference Clock frequency, revised the values. • For the Ethernet Reference Clock added the Frequency in MII/MMII-MAC mode and MII/MMII-MAC mode clock duty cycle parameters. • For the PTP Reference Clock, added the Slew rate and Pk-Pk jitter parameters. 10. Revised Section 8.6.2.1, SDRAM DDR2 Interface AC Timing Table, on page 71, to provide only the AC timing at 200 MHz. 11. In Table 59, Thermal Data for the 88F6180 in the 225-pin LFBGA Package (Preliminary), on page 100, revised the values. 12. In Table 60, LFBGA 225-pin Package Dimensions, on page 102 changed the mold flatness to 0.200 mm from 0.250 mm.
C	August 18, 2008	Revision
		1. Made the following changes throughout this specification: • Added the Audio (S/PDIF / I^2S), SDIO, and Nand Flash interfaces. • Added the Real Time Clock. • Revised the Gigabit Ethernet interface. • Revised the name of the VDD_GE_A pin to VDD_GE. • Increased the number of multi-purpose pins from 11 to 30. • Changed the package to a 225-pin LFBGA package, 13 ×13 mm, 0.8 mm pitch package. 2. Added the XOR engine to the block diagram in the Product Overview on page 3. 3. In the Features list revised the bullet: Up to Up to 200 MHz clock frequency (400 MHz data rate) on page 4. 4. In Figure 1, 88F6180 Pin Logic Diagram, on page 16, added VHV, SSCG_AVSS, and MRn and changed PEX_CLK_P/N for input to input/output (I/O). 5. In Table 3, Power Pin Assignments, on page 19: • Revised the description of VDD_GE to add additional information about RGMII. • Added VHV. • Changed the voltage for XTAL_AVDD from 2.5V to 1.8V. 6. In Table 4, Miscellaneous Pin Assignments, on page 20, added signal MRn. 7. In Table 6, PCI Express Interface Pin Assignments, on page 23, changed PEX_CLK_P/N for input to input/output (I/O). 8. In Table 5, DDR SDRAM Interface Pin Assignments, on page 21, revised the description of M_NCASL and M_PCAL to indicate the range of the resistor. 9. In Table 7, Gigabit Ethernet Port Interface Pin Assignments, on page 24, added a note: For the TXCLK, use the GE_RXCLK pin and added a description for MII/MMII to the GE_TXD[3:0], GE_TXCTL, GE_RXCTL, GE_RXCLK, GE_RXD[3:0] rows. 10. Revised Table 8, Serial Management Interface (SMI) Pin Assignments, on page 26. 11. In Table 13, MPP Interface Pin Assignment, on page 31, revised the description of MPP[35]. 12. Revised Table 18, Secure Digital Input/Output (SDIO) Interface Signal Assignment, on page 36 to indicate the pins requiring pull up. 13. Added Section 1.2.17, Precise Timing Protocol (PTP) Interface, on page 37. 14. In Table 20, Internal Pull-up and Pull-down Pins, on page 38, revised the pin numbers and changed pins GE_MDC and MPP[7] from pull down to pull up and added NF_ALE, NF_REn, NF_CLE, NF_CEn, and NF_WEn. 15. Revised Table 25, 88F6180 Clocks, on page 46 and Table 26, Supported Clock Combinations, on page 47.

Table 62: Revision History (Continued)

Revision	Date	Comments
16. In Section 4.1, Multi-Purpose Pins Functional Summary, on page 41: • Changed all references to MPP[0] from GPI to GPIO. • Changed the MPP[6] row in the table to remove the 0x0 option. • Added the following bullets at the end of the section, after the table: - When TWSI serial ROM initialization is enabled, MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively. - Pin MPP[6] wakes up after reset in 0x1 mode (SYSRST_OUTn). - The UART0 or UART1 signals must not be configured to more than one MPP. • Revised the description of SYSRST_OUTn. • In the notes following the table, changed the description for wake up of MPP[7].		
17. Added Section 4.2, Gigabit Ethernet (GbE) Pins Multiplexing on MPP, on page 45.		
18. In Table 25, 88F6180 Clocks, on page 46, revised the PEX PHY and USB PHY PLL rows and added the PTP clock. Also changed references to the Core clock to be the TCLK.		
19. Revised the supported clock combinations in Table 26, Supported Clock Combinations, on page 47. Also revised the values in the ratio columns so they appear as rations.		
20. Revised Section 5.1, Spread Spectrum Clock Generator (SSCG), on page 47.		
21. In Table 28, Reset Configuration, on page 52, revised the configuration function of TWSI Serial ROM Initialization to indicate that MPP[8] and MPP[9] wake up as TWSI data and clock pins, respectively.		
22. Revised Table 27, I/O and Core Voltages, on page 48.		
23. In Section 6.2, Hardware Reset, on page 49, added SYSRST_OUTn to the list of pins that are still active during SYSRSTn assertion.		
24. Revised Section 6.2.1, Reset Out Signal, on page 50 and Section 6.2.3, SYSRSTn Duration Counter, on page 50 and added Section 6.2.2, Power On Reset (POR), on page 50.		
25. In Section 6.3.2, PCI Express Endpoint Reset, on page 51 revised the bulleted items.		
26. Revised Section 6.5, Pins Sample Configuration, on page 51.		
27. Made major revisions to Table 28, Reset Configuration, on page 52.		
28. Revised the first two paragraphs in Section 6.6, Serial ROM Initialization, on page 54.		
29. In Section 6.7, Boot Sequence, on page 55 added step 4: If configured to boot from NAND flash (and BootROM is disabled), the device also performs a NAND Flash boot sequence to prepare page 0 in the NAND flash device for read. Also revised the paragraph following step 4.		
30. In Table 30, IDCODE Register Map, on page 58, revised the description of bits [31:28].		
31. Deleted Section 8.5.2 REF_CLK_XIN 2.5V (CMOS) DC Electrical Specifications and added pin REF_CLK_XIN to Section 8.5.2, RGMII, SMI and REF_CLK_XIN 1.8V (CMOS) DC Electrical Specifications, on page 66, since the power rail for the REF_CLK_XIN pin was changed from 2.5V to 1.8V.		
32. In Table 31, Absolute Maximum Ratings, on page 59: • Added VHV. • Revised the voltage for and XTAL AVDD. • Revised the description of the VDD_GE row to add MII/MMI to the row for 3.3V VDD_GE description.		
33. In the Table 32, Recommended Operating Conditions, on page 61: • Added VHV. • Revised the voltage for and XTAL AVDD. • Added values for VDD_CPU. • For the 3.3V interfaces, revised the minimum value to 3.15V and the maximum value to 3.45V (+/-5%). • Revised the description of the VDD_GE row, to show that RGMII can also operate with a voltage of 3.3V. • Added MII/MMII to the row for 3.3V VDD_GE description and indicated that for both 1.8V and 3.3V, this pin supports both RGMII and SMI. • Revised the values for PEX_AVDD to minimum 1.7V, typical 1.8V, and maximum 1.9V.		

Table 62: Revision History (Continued)

Revision	Date	Comments
34. In Table 33, Thermal Power Dissipation, on page 63: • Revised the values for the parameter *Core (including CPU)*. • Revised the interface *RGMII 1.8V interface* to *RGMII 1.8V or 3.3V interface*. • Added the row for the MII/MMII 3.3V interface. • Revised the interface description for parameter P_{DDR2}. • Revised values for Core, PCI Express, and USB parameters. • Revised the notes following the table, to remove reference to the trace length or resistance.		
35. In Table 34, Current Consumption, on page 64: • Revised the values for the parameter *Core (including CPU)*. • Revised the interface *RGMII 1.8V interface* to *RGMII 1.8V or 3.3V interface*. • Added the row for the MII/MMII 3.3V interface. • Revised the interface description for parameter I_{DDR2}. • Revised values for the PCI Express and USB parameters. • Revised the notes following the table, to remove reference to the trace length or resistance. • For the 3.3V interfaces, revised the minimum value to 3.15V and the maximum value to 3.45V (+/-5%).		
36. In Section 8.5.1, General 3.3V (CMOS) DC Electrical Specifications, on page 65, added reference to PTP, RGMII and MMI/MMII.		
37. Revised Table 40, Reference Clock AC Timing Specifications, on page 69.		
38. Revised the title of Table 41, SDRAM DDR2 Interface AC Timing Table, on page 71 and added Table 42, SDRAM DDR2 Interface AC Timing Table (Two Chip Selects), on page 159, to provided SDRAM AC values when using one or two chip selects.		
39. Add Section Table 43:, RGMII 10/100 AC Timing Table at 3.3V, on page 74.		
40. Add Section 8.6.4, Media Independent Interface/Marvell Media Independent Interface (MII/MMII) AC Timing, on page 76.		
41. Revised Table 53, PCI Express Interface Differential Reference Clock Characteristics, on page 92 and Table 54, PCI Express Interface Spread Spectrum Requirements, on page 93.		
42. Revised Figure 22, TWSI Output Delay AC Timing Diagram, on page 83, to show SDA t_{ov} relative to the SCK falling edge, as it appears in the two tables preceding the figure.		
43. Revised the values in Table 59, Thermal Data for the 88F6180 in the 225-pin LFBGA Package (Preliminary), on page 100.		
44. Revised all of Section 10, Package, on page 101 and Section 11, Part Order Numbering/Package Marking, on page 103.		
B	April 8, 2008	Revision
1. In the features list: • Added the bullets Precise Timing Protocol (PTP) and Audio Video Bridging networks on page 5. • Added the functional block diagram and the usage model diagram. • Revised the bullet describing the package type and size on page 9.		
2. Throughout this specification, LVCMOS and LVTTL were changed to CMOS.		
3. In Table 1, 88F6180 Pin Logic Diagram, on page 16 added SSGC_VDD to the power pins and removed the interfaces that are multiplexed on the MPP pins.		
4. Revised Table 1, Pin Functions and Assignments Table Key, on page 17 to show only terms relevant for this device.		
5. In Table 3, Power Pin Assignments, on page 19, added pin SSCG_AVDD and added the SMI interface at 1.8V and the MII/MMII interface at 3.3V to the description of the interfaces supported by pin VDD_GE_A. Also revised the description of VDD to indicate that it provides the CPU voltage.		
6. Revised all of the pin numbers in Table 20, Internal Pull-up and Pull-down Pins, on page 38.		
7. In Table 7, Gigabit Ethernet Port Interface Pin Assignments, on page 24, removed pins GE_MDC and GE_MDIO.		
8. Added Section 1.2.6, Serial Management Interface (SMI) Interface Pin Assignments, on page 26, with a description of the GE_MDC and GE_MDIO pins.		

Table 62: Revision History (Continued)

Revision	Date	Comments
		9. In Table 14, Two-Wire Serial Interface (TWSI) Interface Pin Assignment, on page 32, changed the note to: Requires a pull-up resistor to VDDO.
		10. Added Section 2, Unused Interface Strapping, on page 39.
		11. In Figure 2, 88F6180 Pin Map Top View[88F6180], on page 40 and Table 22, 88F6180 Pinout Sorted by Pin Number[88F6180], on page 41, reorganized the pinout to: • Add pin SSCG_VDD as pin 66. • Remove pin XTAL_VSS. • Changed the function of the following pins: 1–67, 69–78, 80–103, 108–128. • Changed the name of the ODT pin from M_ODT[0] to M_ODT.
		12. In Table 25, 88F6180 Clocks, on page 46, revised the description of CPU PLL to mention SSCG.
		13. Added Section 5.1, Spread Spectrum Clock Generator (SSCG), on page 47.
		14. Added Section 6.1, Power-Up/Down Sequence Requirements, on page 48 and revised the title of Section 6 to reflect this change.
		15. In Section 6.4, Sheeva™ CPU TAP Controller Reset, on page 51, revised the note referring to sample at reset and added the note: If a signal is pulled up on the board, it must be pulled to proper voltage level. Certain reset configuration pins are powered by VDD_GE_A. That pin has multiple voltage options (see Table 32, Recommended Operating Conditions, on page 61).
		16. In Table 28, Reset Configuration, on page 52added the following note to the description of the GE_MDC pin: Internally pulled to 0x0.
		17. In Table 31, Absolute Maximum Ratings, on page 59 and Table 32, Recommended Operating Conditions, on page 61, changed VDD_CPU to VDD and added the parameter SSCG_VDD.
		18. In Table 33, Thermal Power Dissipation, on page 63 added the following: *The purpose of the Thermal Power Dissipation table is to support system engineering in thermal design*. Also changed VDD_CPU to VDD.
		19. In Table 34, Current Consumption, on page 64 added the following: *The purpose of the Current Consumption table is to support board power design and power module selection*. Also changed VDD_CPU to VDD.
		20. In Table 40, Reference Clock AC Timing Specifications, on page 69: • Revised the symbols for the SMI master mode reference clock. • Revised the symbols for the TWSI master mode reference clock. • Removed the RGMII rows from this table since they are not relevant to this device.
		21. In Table 65, Thermal Data for the 88F6180 (Preliminary), on page 102, added values for all of the parameters.
A	January 28, 2008	Initial release

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